

ZZZ1
LA5972P_LS5971P_LS5083P

ZZZ3
LA5972P
DAZ@

ZZZ4
LS5971P
DAZ@

ZZZ5
LS5083P
DAZ@

Compal Confidential

NAWA2 Schematics Document

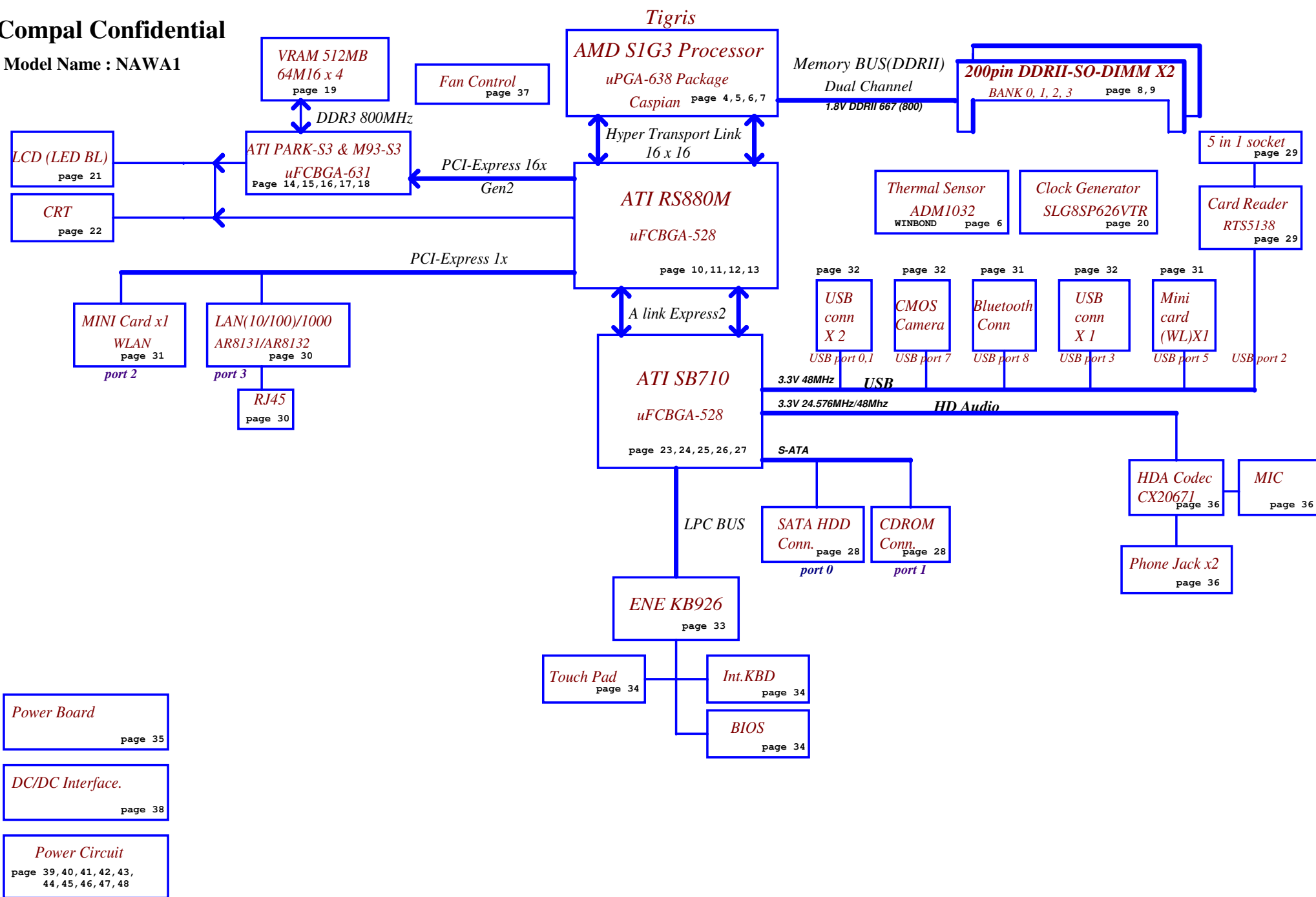
AMD Tigris: Caspian Processor with RS880M/SB710/Park-S3 & M93-S3

2009-11-26

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Model Name : NAWA1



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

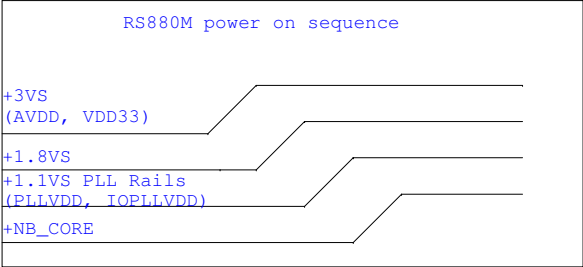
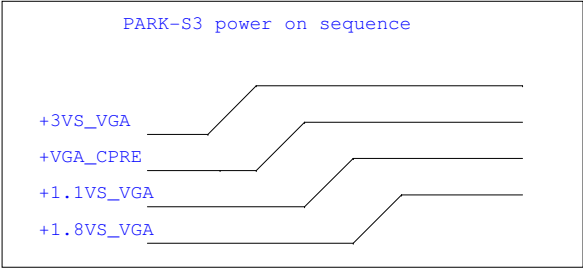
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
PARK	PARK@
M93	M93@
HDT debug	HDT@
UMA	UMA@
Wireless LAN	WLAN@
Blue Tooth	BT@
Camera	CMOS@
New Card	New Card@
VRAM	X76@
UNPON	@

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

NAWA1_UMA : UMA@/WLAN@/BT@/CMOS@/NEW_CARD@
NAWA1_DIS : VGA@/M93@/WLAN@/BT@/NEW_CARD@/CMOS@/X76@



External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
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EC SM Bus1 address

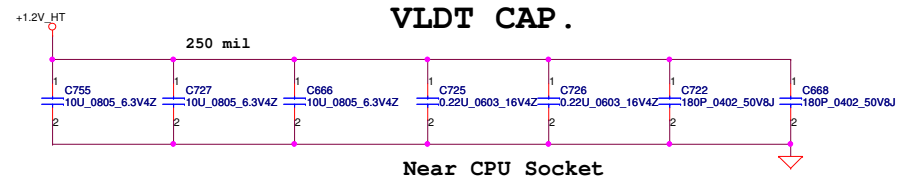
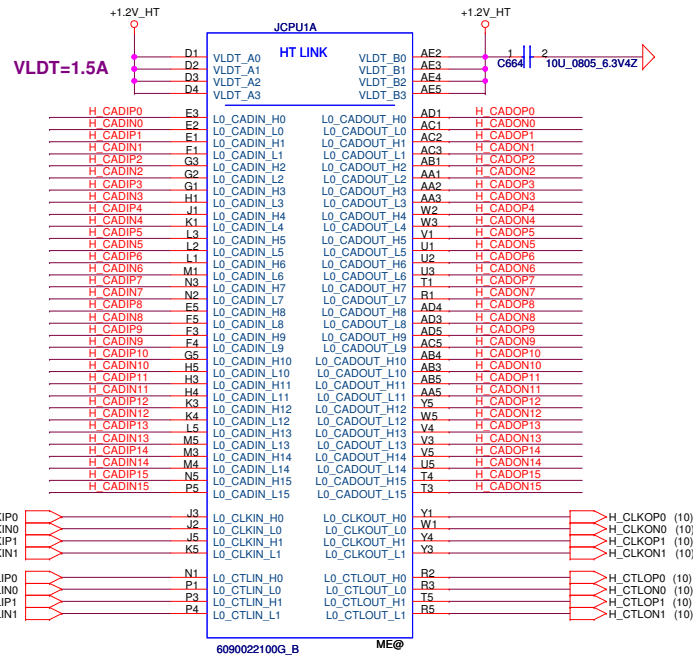
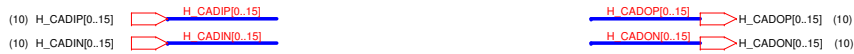
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			GMT G781-1 (GPU)	1001 101X b	9AH
			SB-Temp Sensor		9CH

EC SM Bus2 address

SB710
SM Bus 0 address

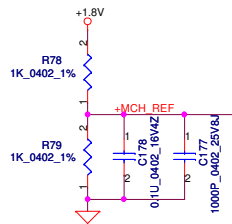
Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2	New card	
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

SB710
SM Bus 1 address

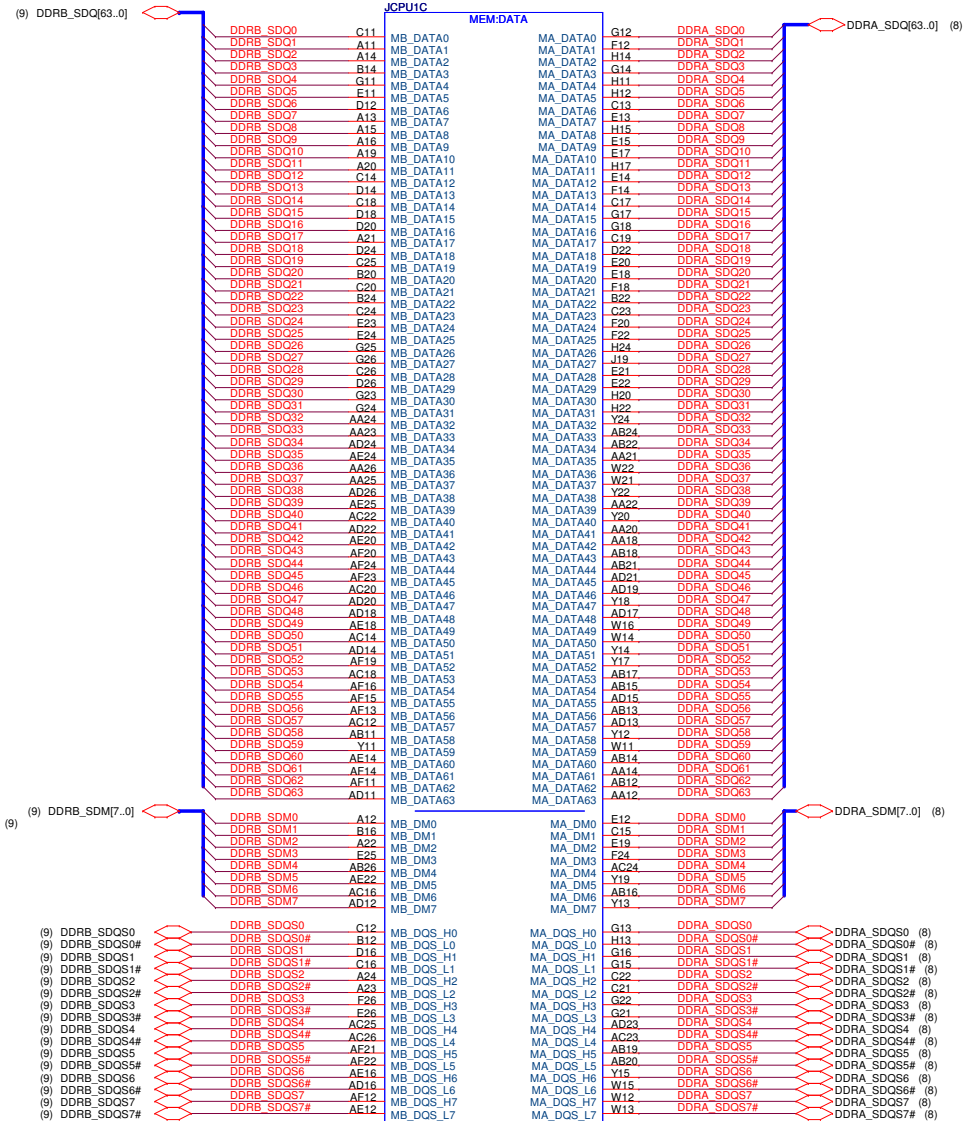
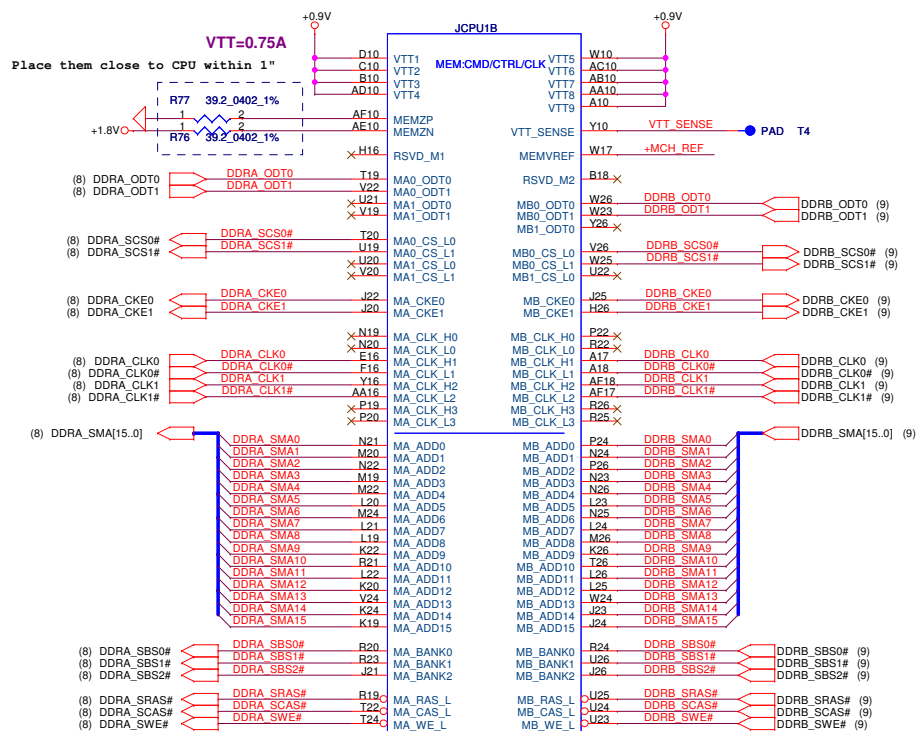
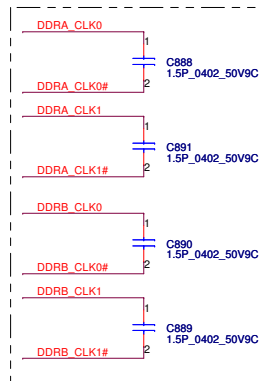


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Processor DDR2 Memory Interface



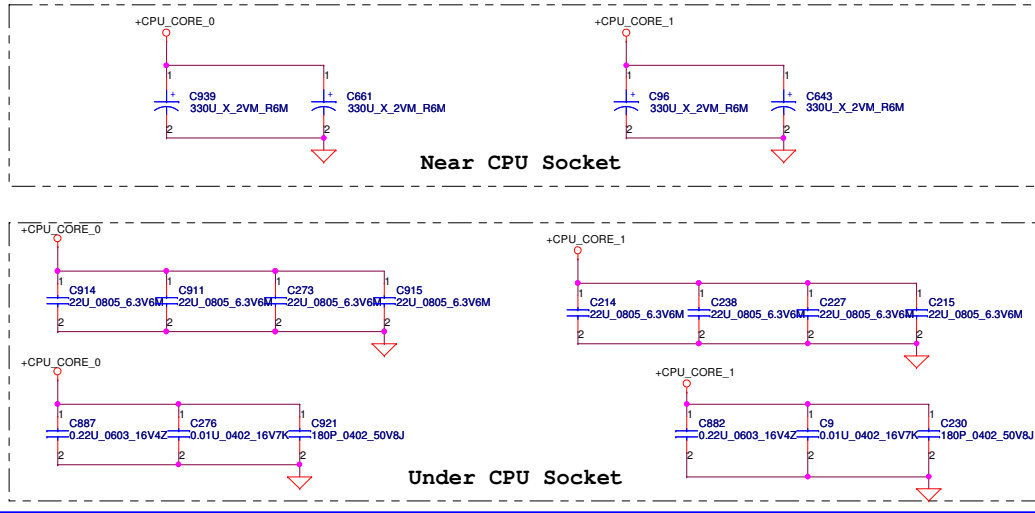
**PLACE CLOSE TO PROCESSOR
WITHIN 1.2 INCH**



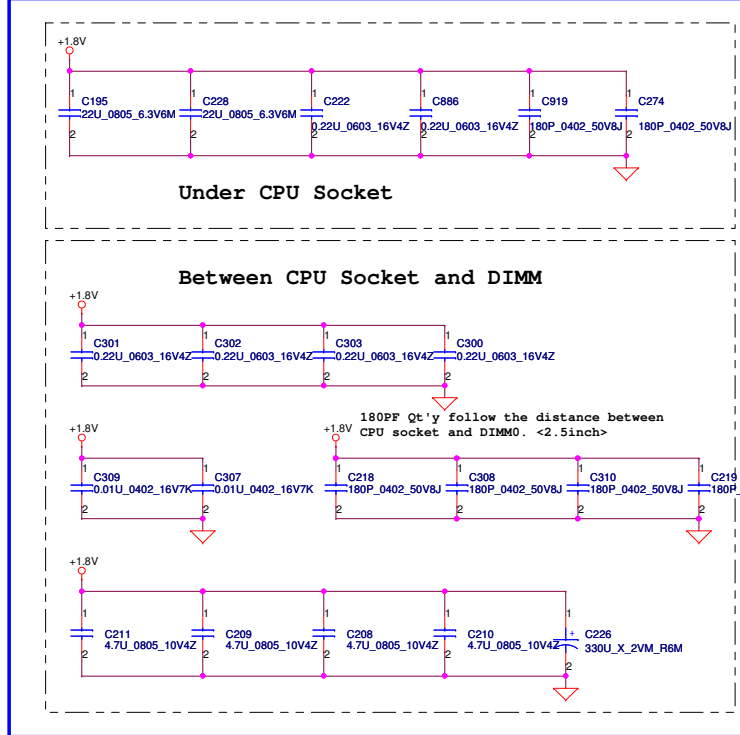


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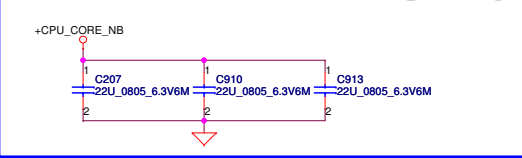
VDD (+CPU_CORE) decoupling.



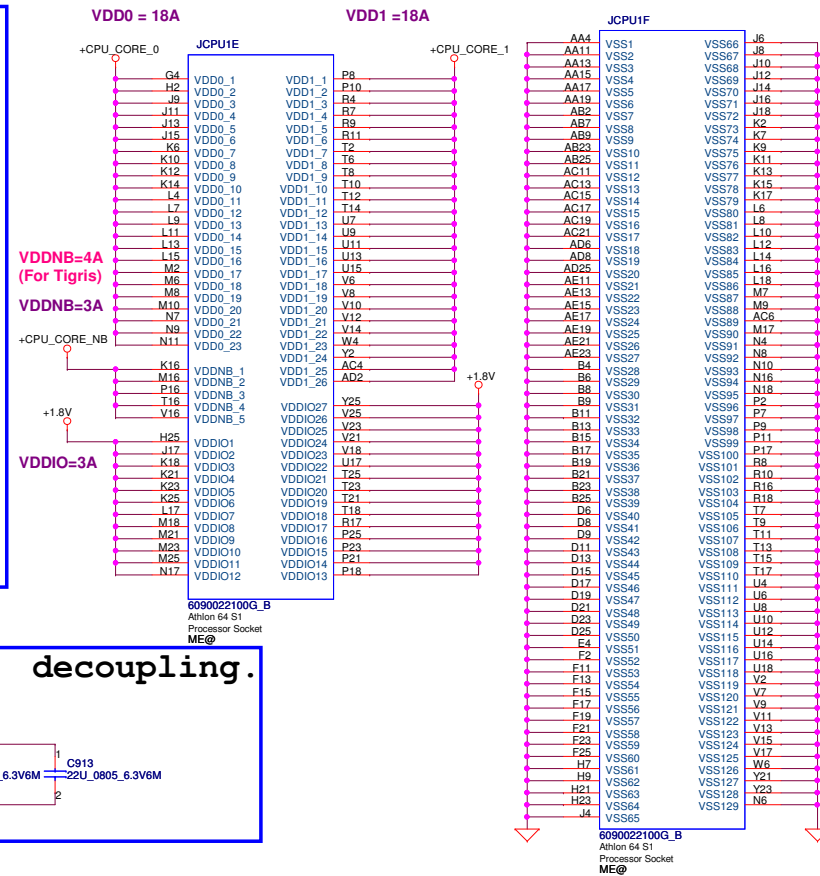
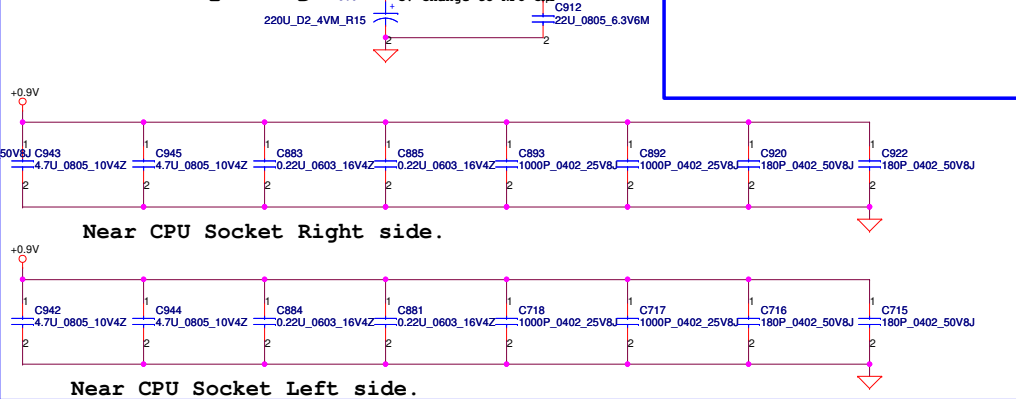
VDDIO decoupling.



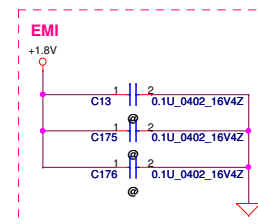
+CPU_CORE_NB decoupling.



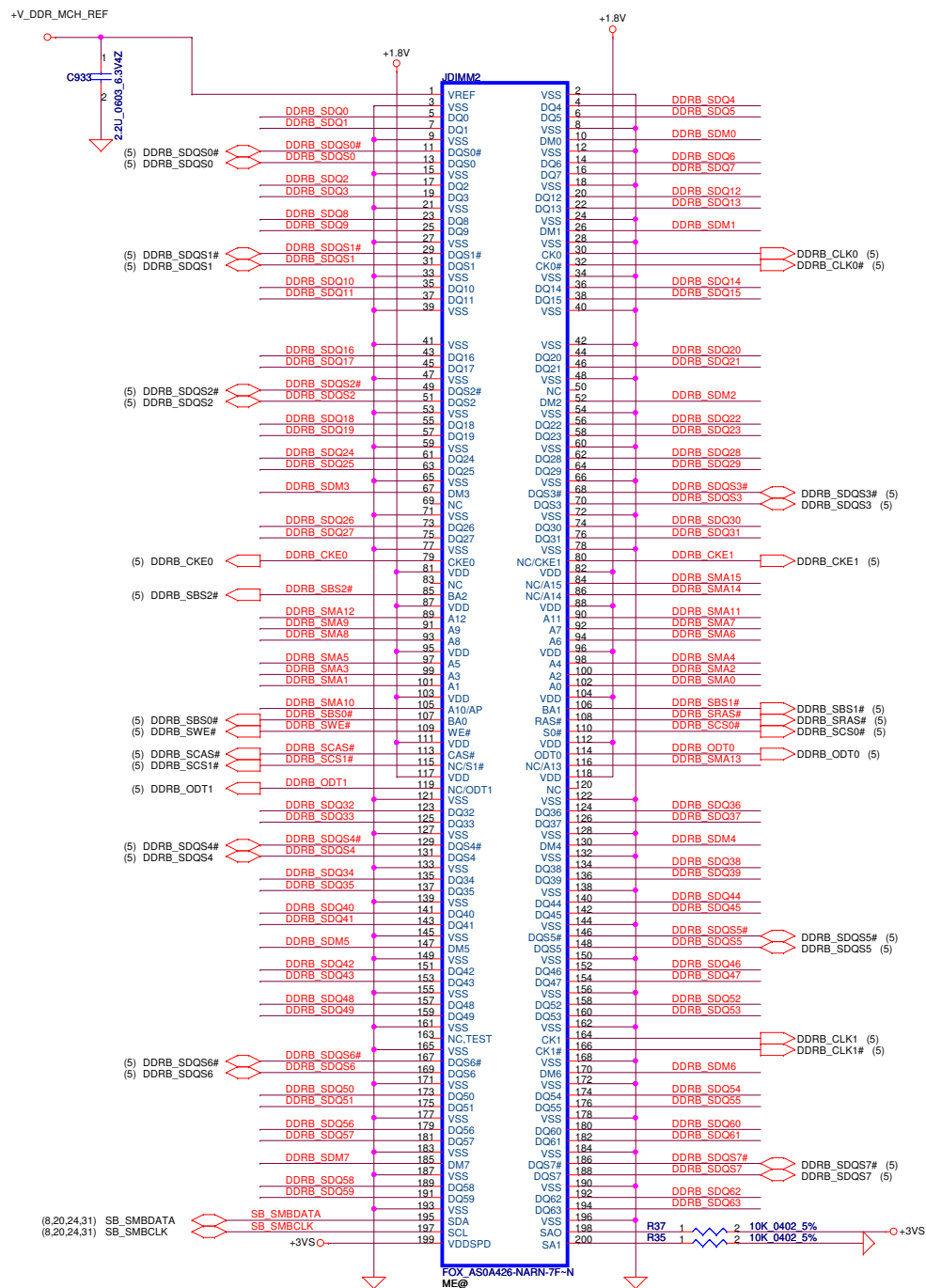
VTT decoupling.

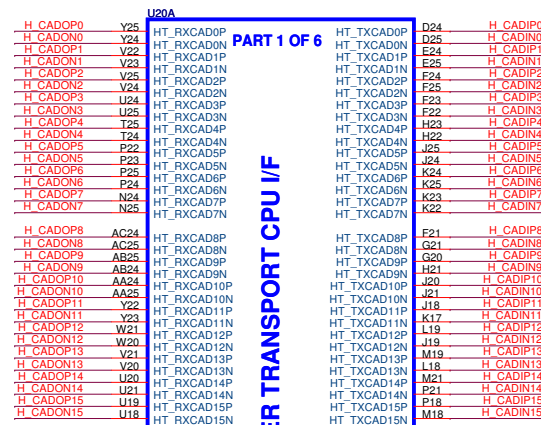
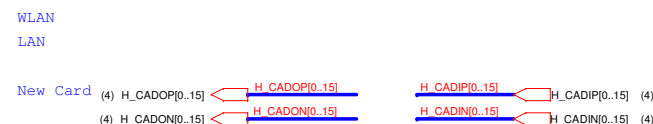
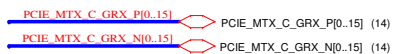


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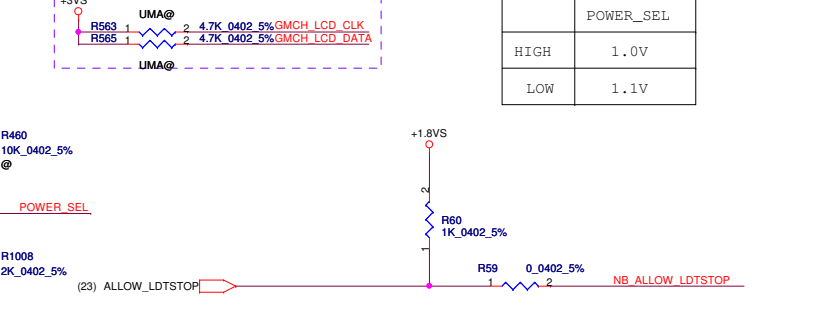
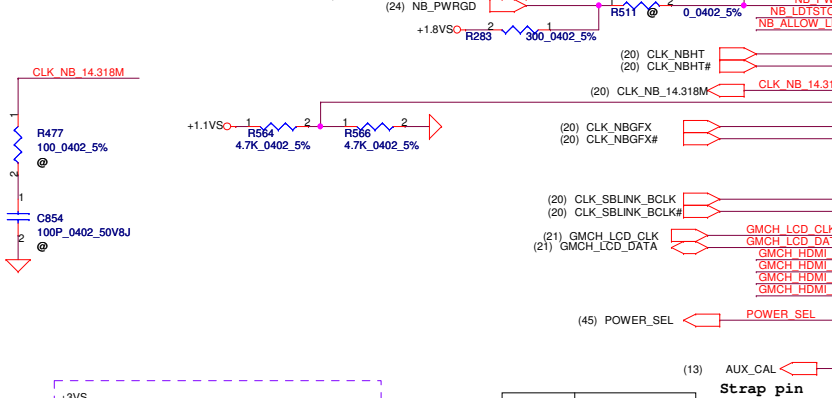
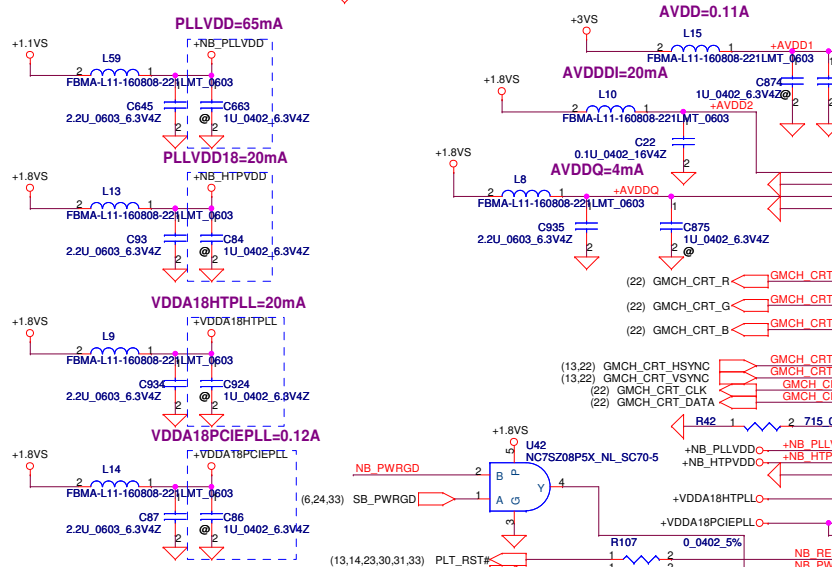
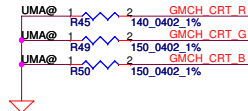
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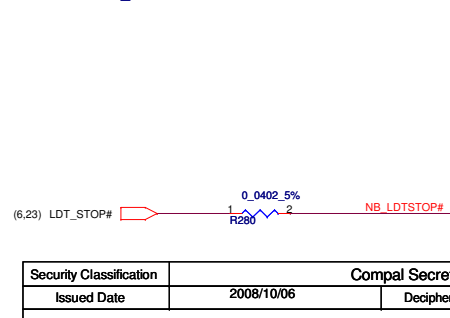
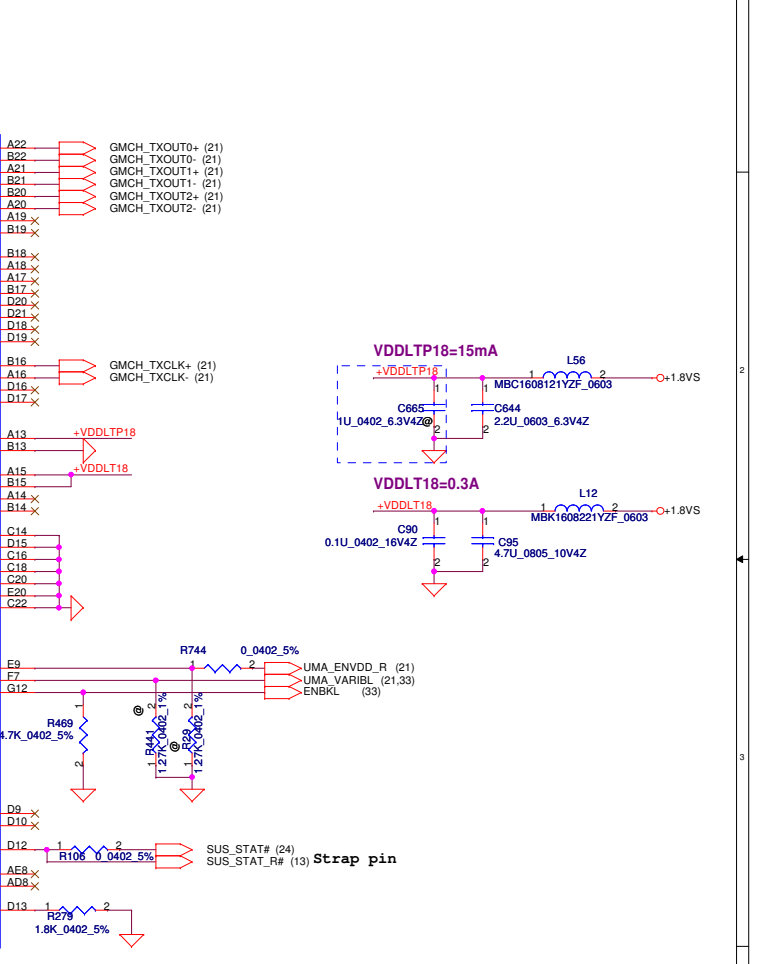
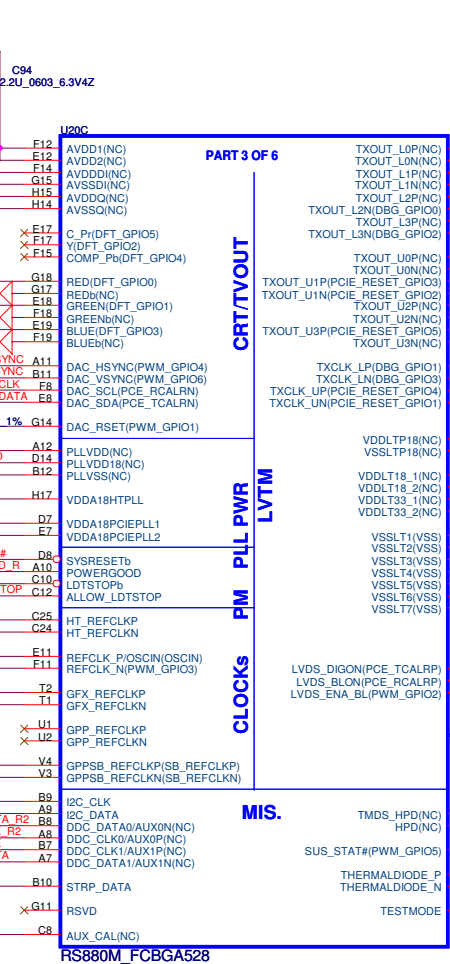


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For RS780M A13
RED: Connected to GND through two separate 140ohm 1% resistor



	POWER_SEL
HIGH	1.0V
LOW	1.1V

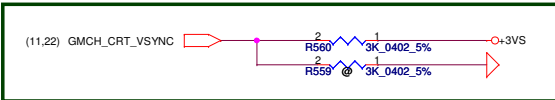


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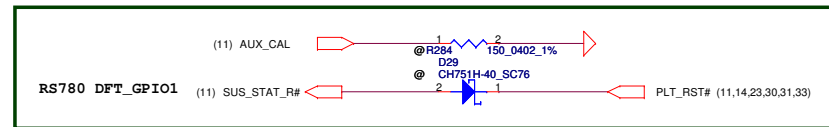


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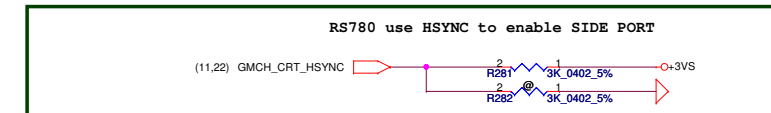
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS880M)
0 : Enable (RS880M)



DFT_GPIO1:LOAD_EEPROM_STRAPS

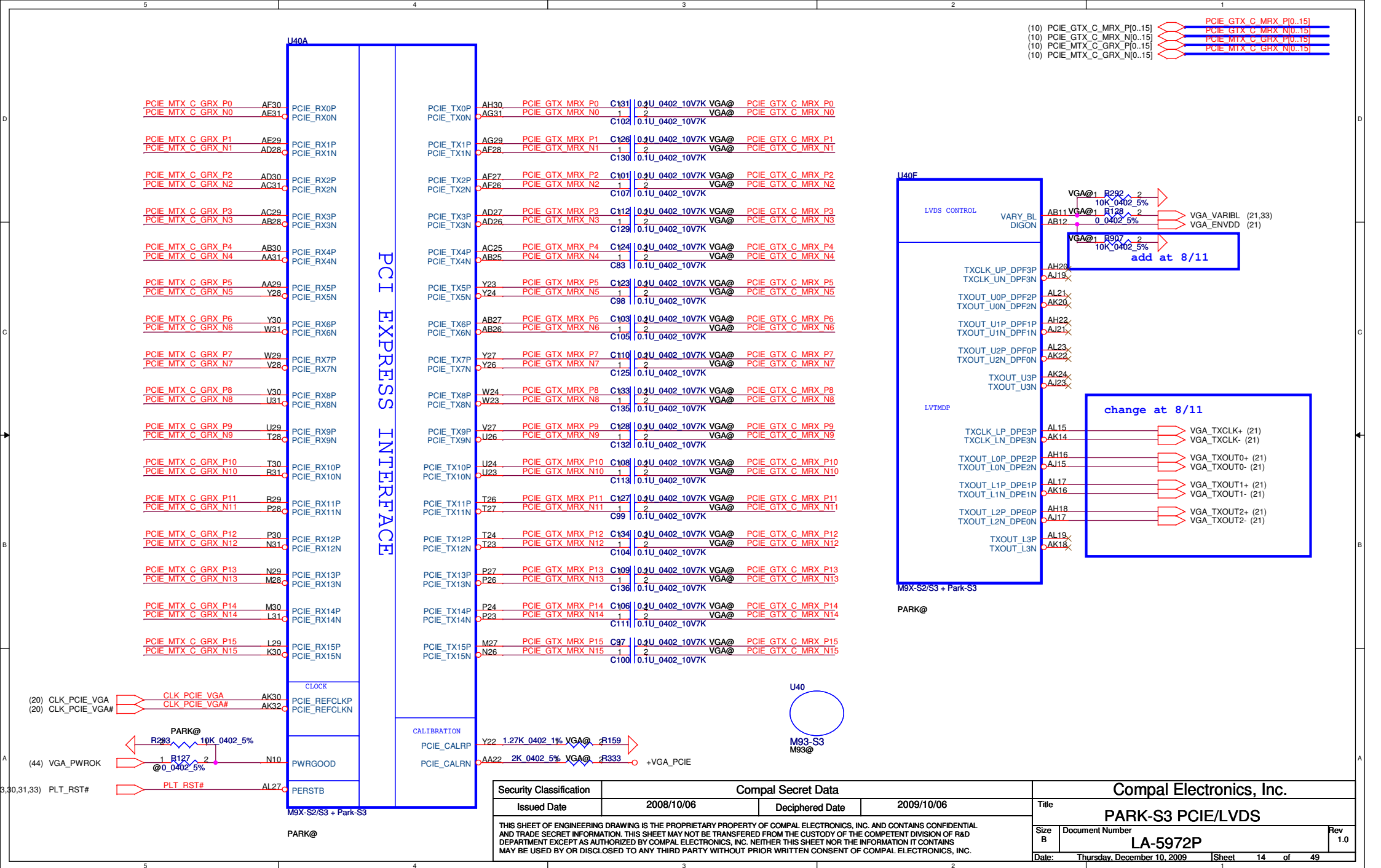
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

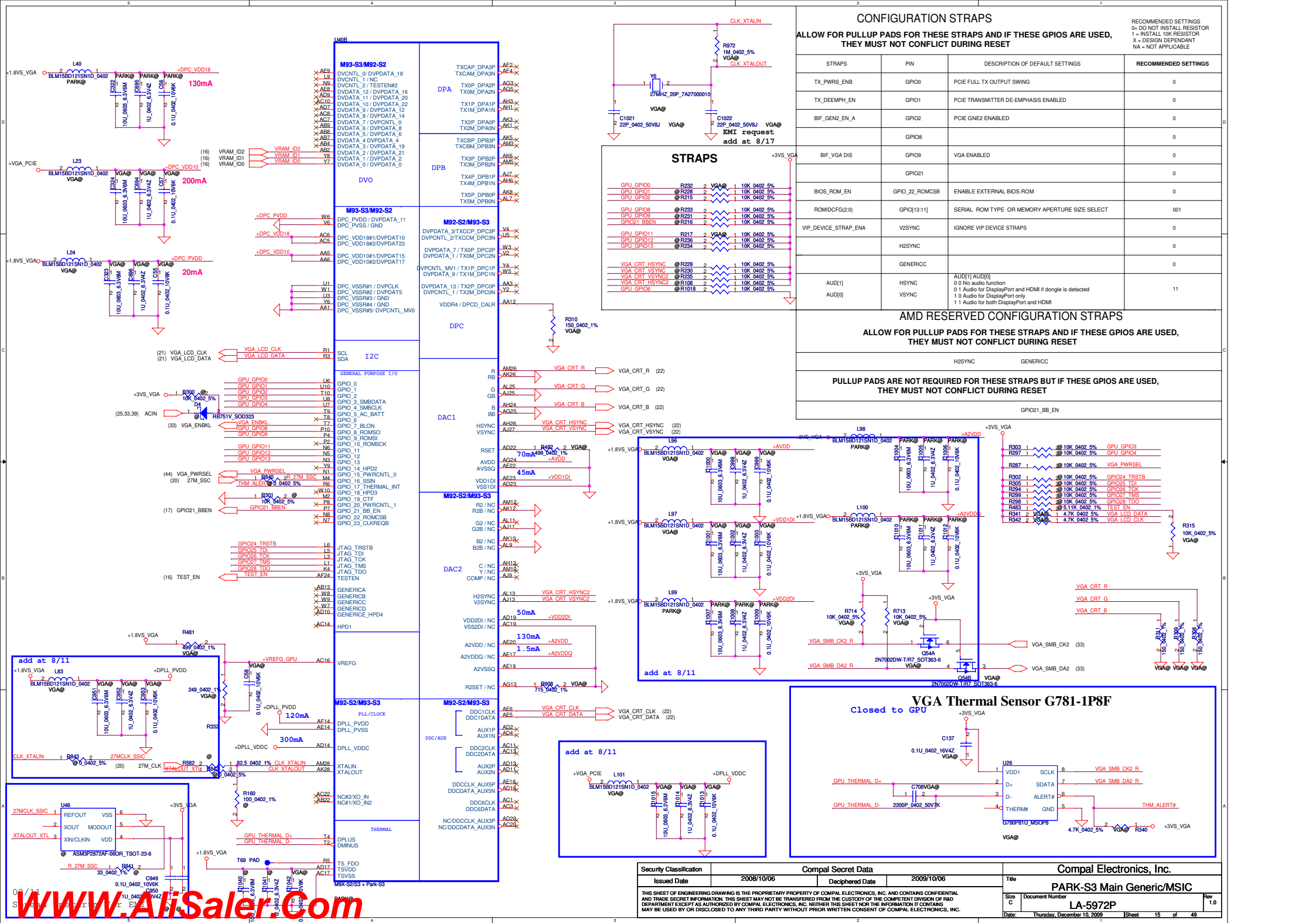


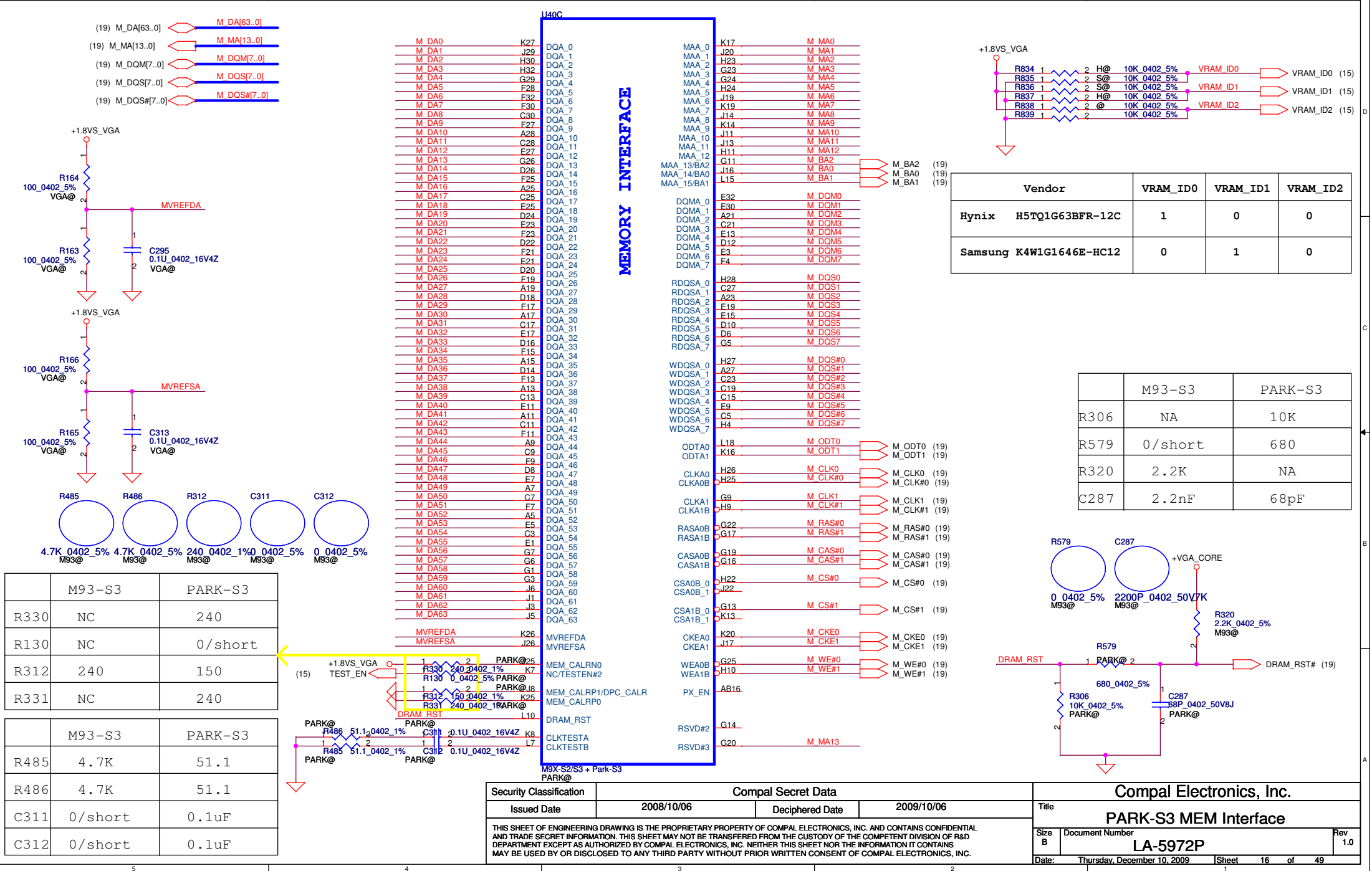
RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0 : Enable (RS880M)
1 : Disable(RS880M)

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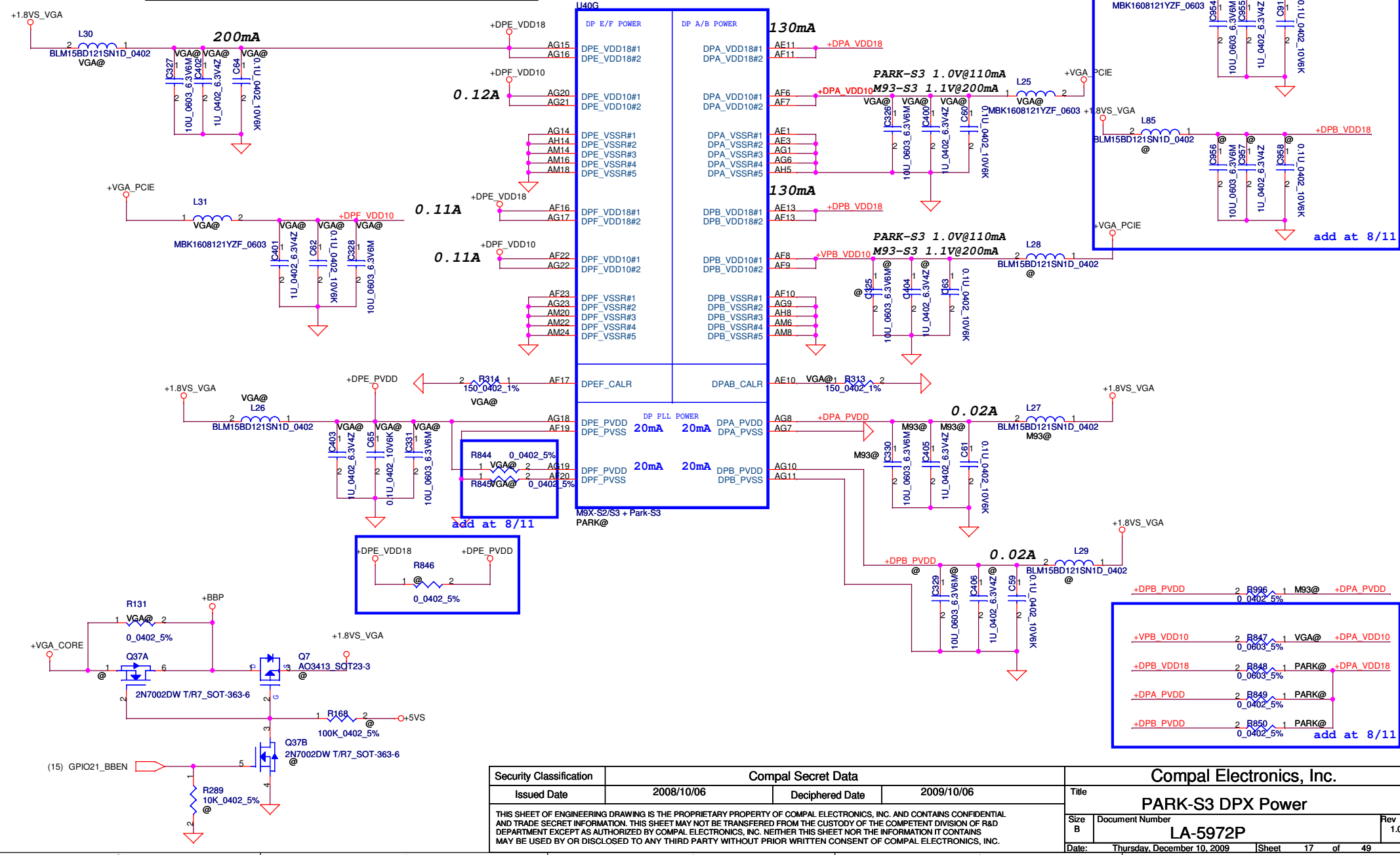




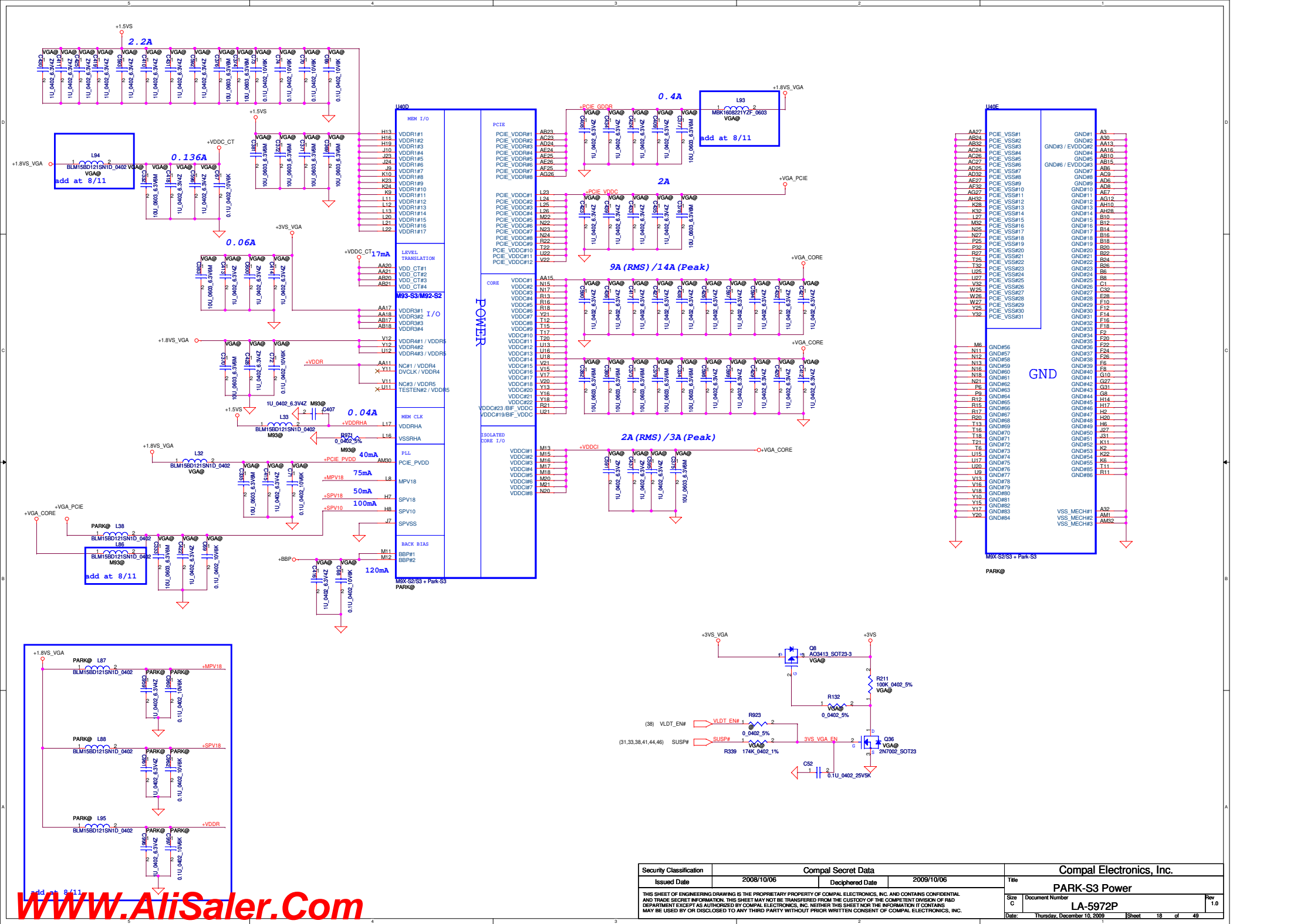



DPE_VDD10
DPF_VDD10

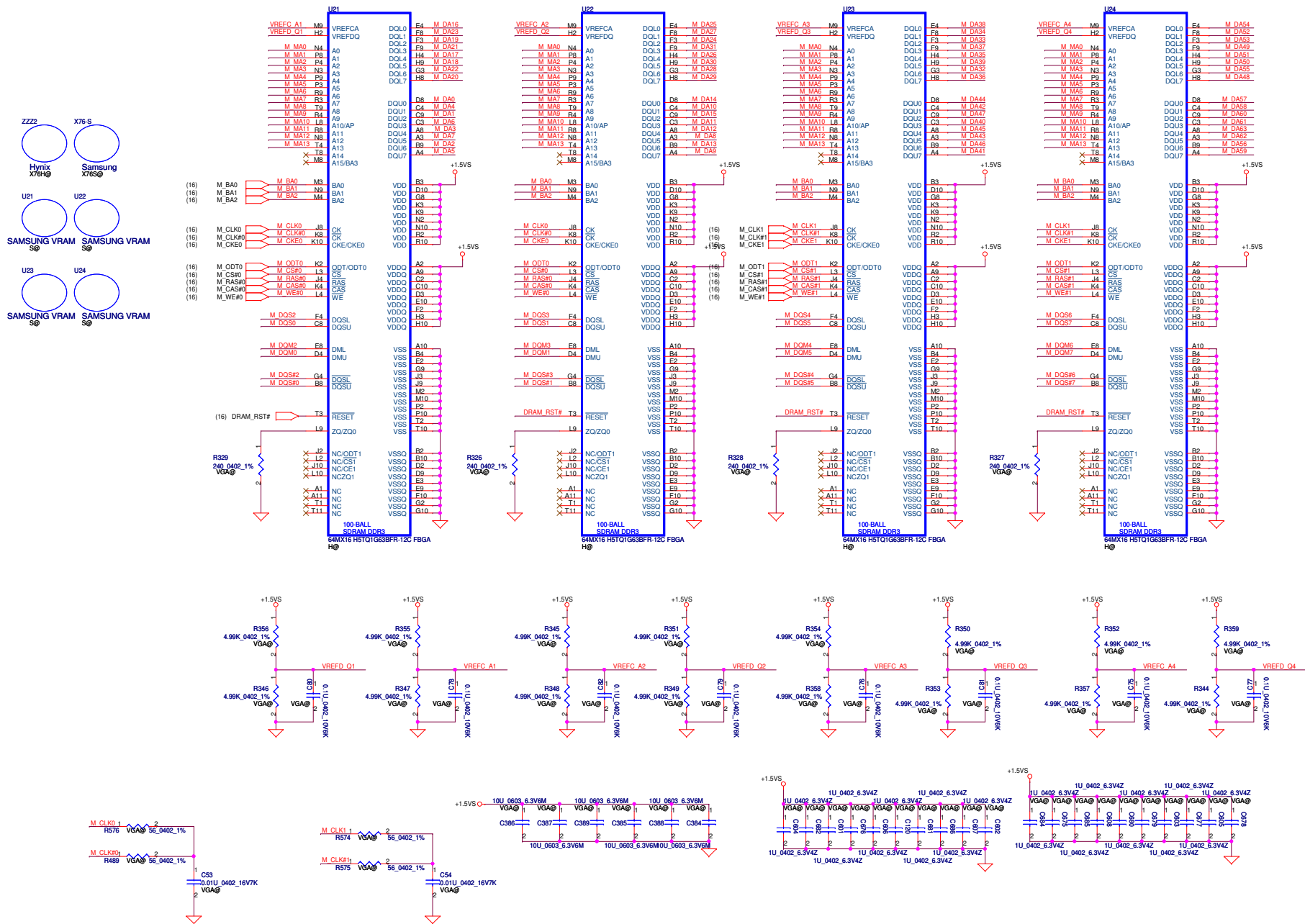
Park-S3: TMDS/DP=110mA@1.0V : LVDS=120mA@1.0V
M9X-S2/S3: TMDS/DP=170mA@1.1V LVDS=100mA@1.1V



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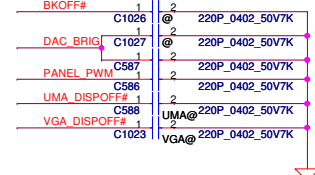
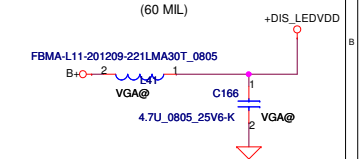
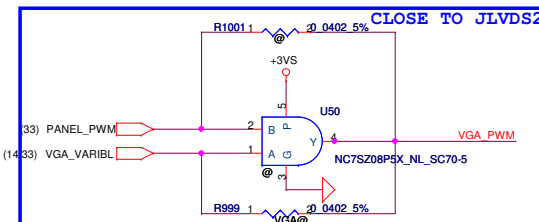
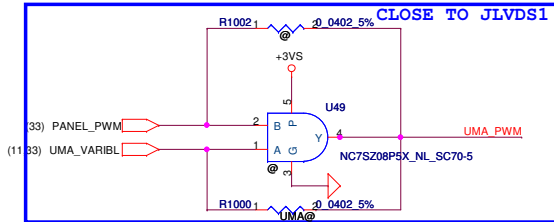
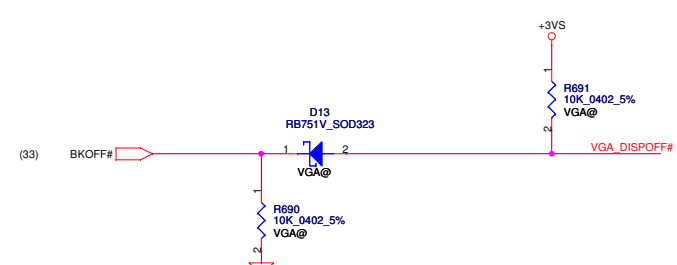
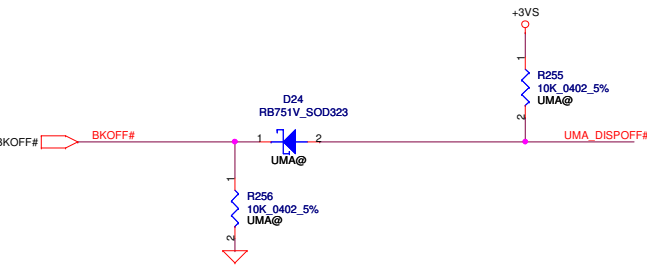
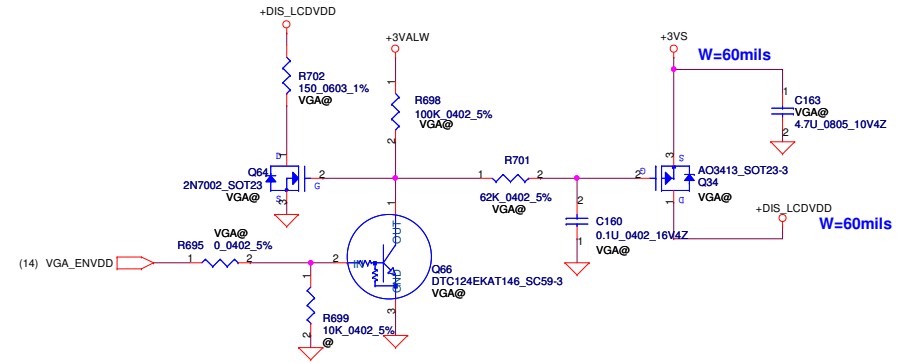
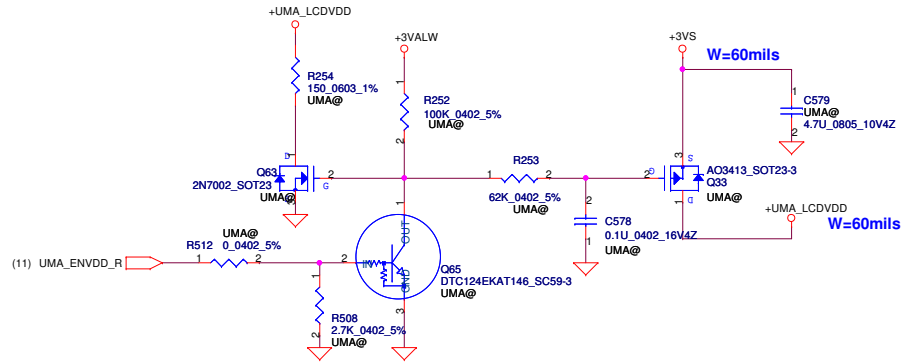


- (16) M_DA[63..0]  M_DA[63..0]
- (16) M_MA[13..0]  M_MA[13..0]
- (16) M_DQM[7..0]  M_DQM[7..0]
- (16) M_DQS[7..0]  M_DQS[7..0]
- (16) M_DQS[7..0]  M_DQS[7..0]

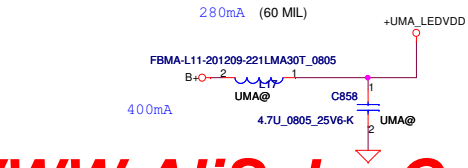
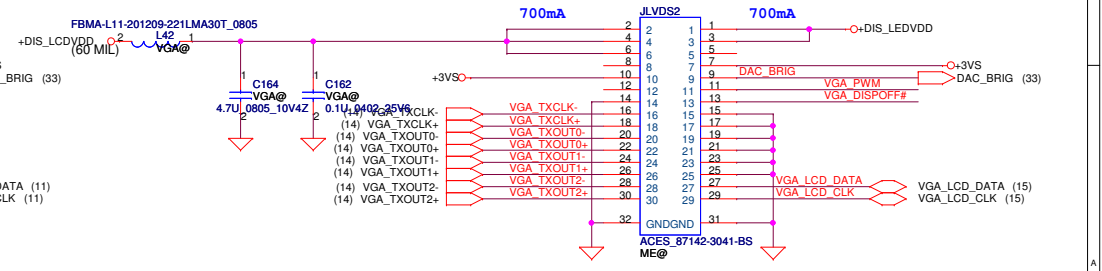
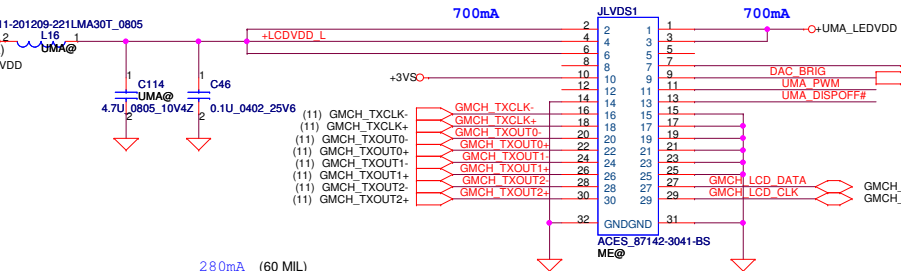


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LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

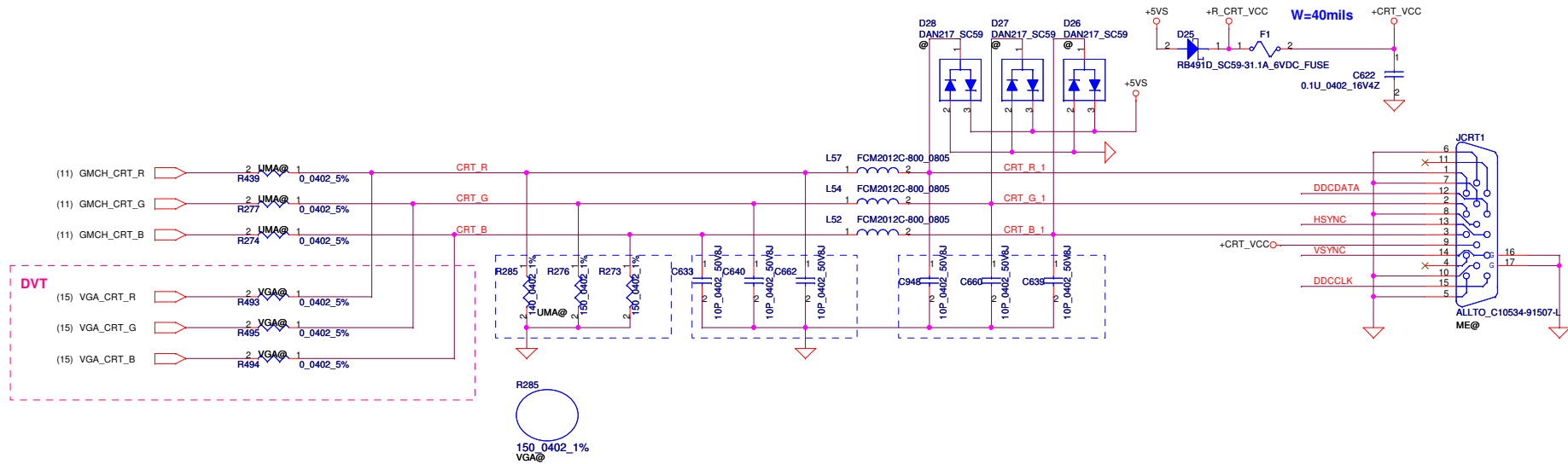


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				Deciphered Date				LVDS Connector			
				2009/10/06				LA-5972P			
Size B				Document Number				Rev 1.0			
Date				Thursday, December 10, 2009				Sheet 21 of 49			

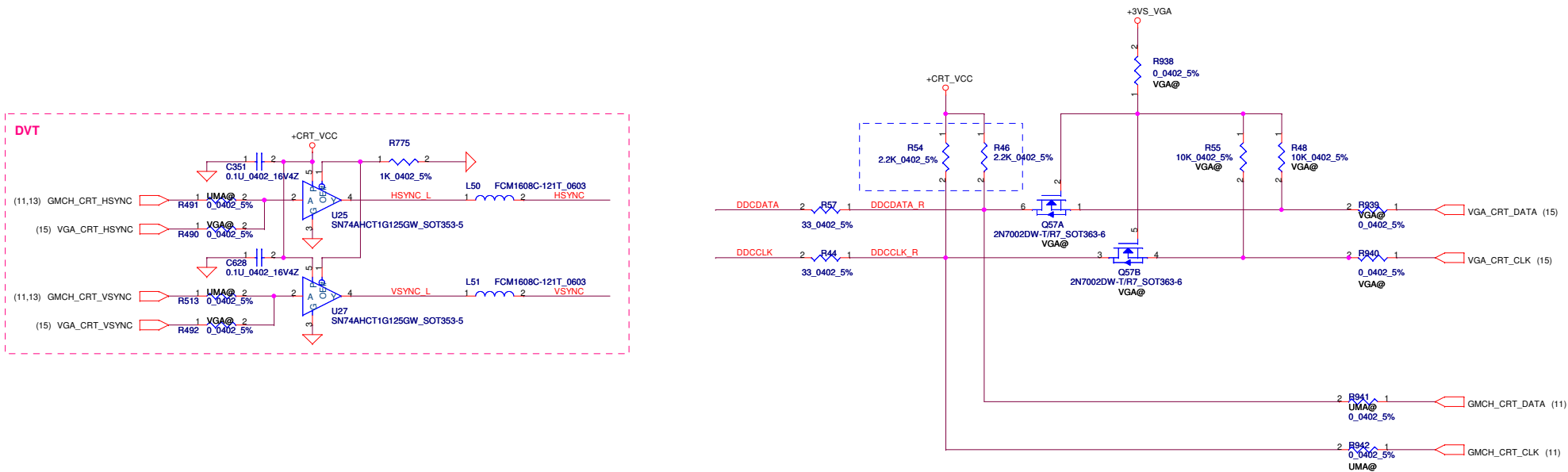
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CRT CONNECTOR



Place closed to chipset

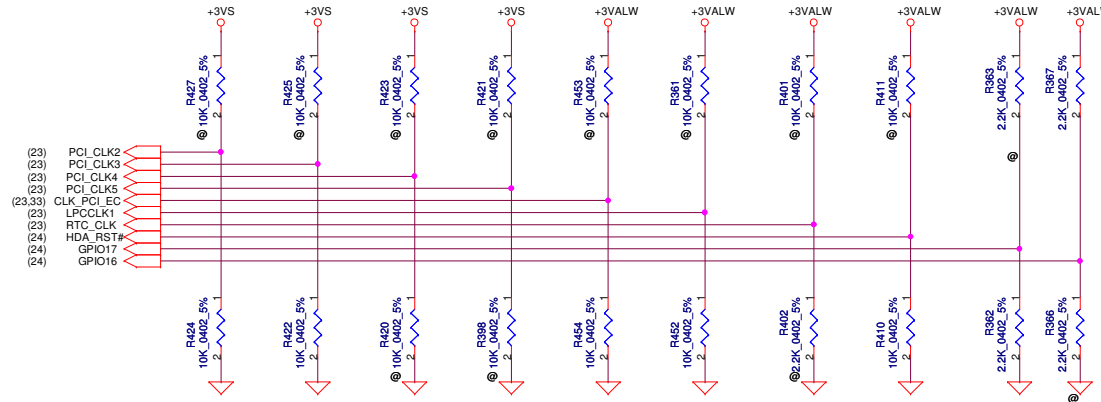


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								CRT Connector			
								Size B			
								Document Number			
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

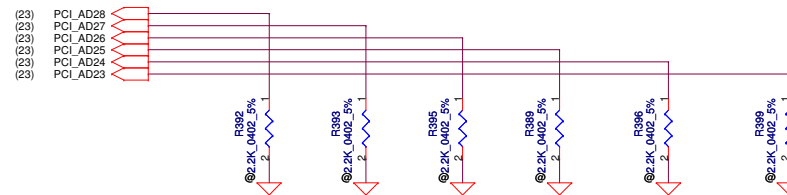
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



DEBUG STRAPS

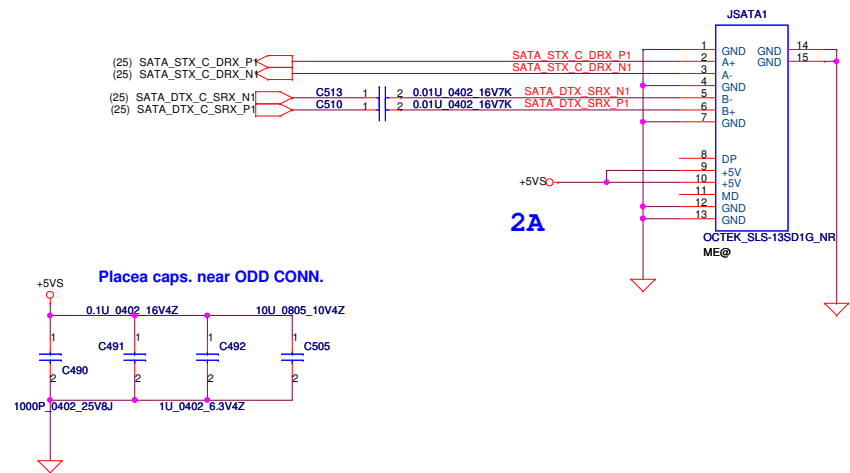
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

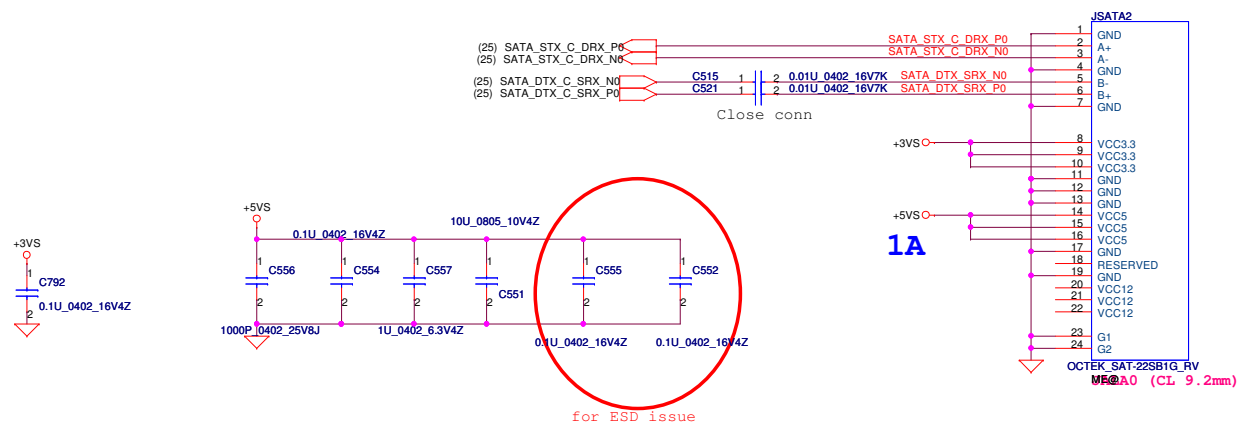


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				Size Custom	Rev 1.0
				LA-5972P	
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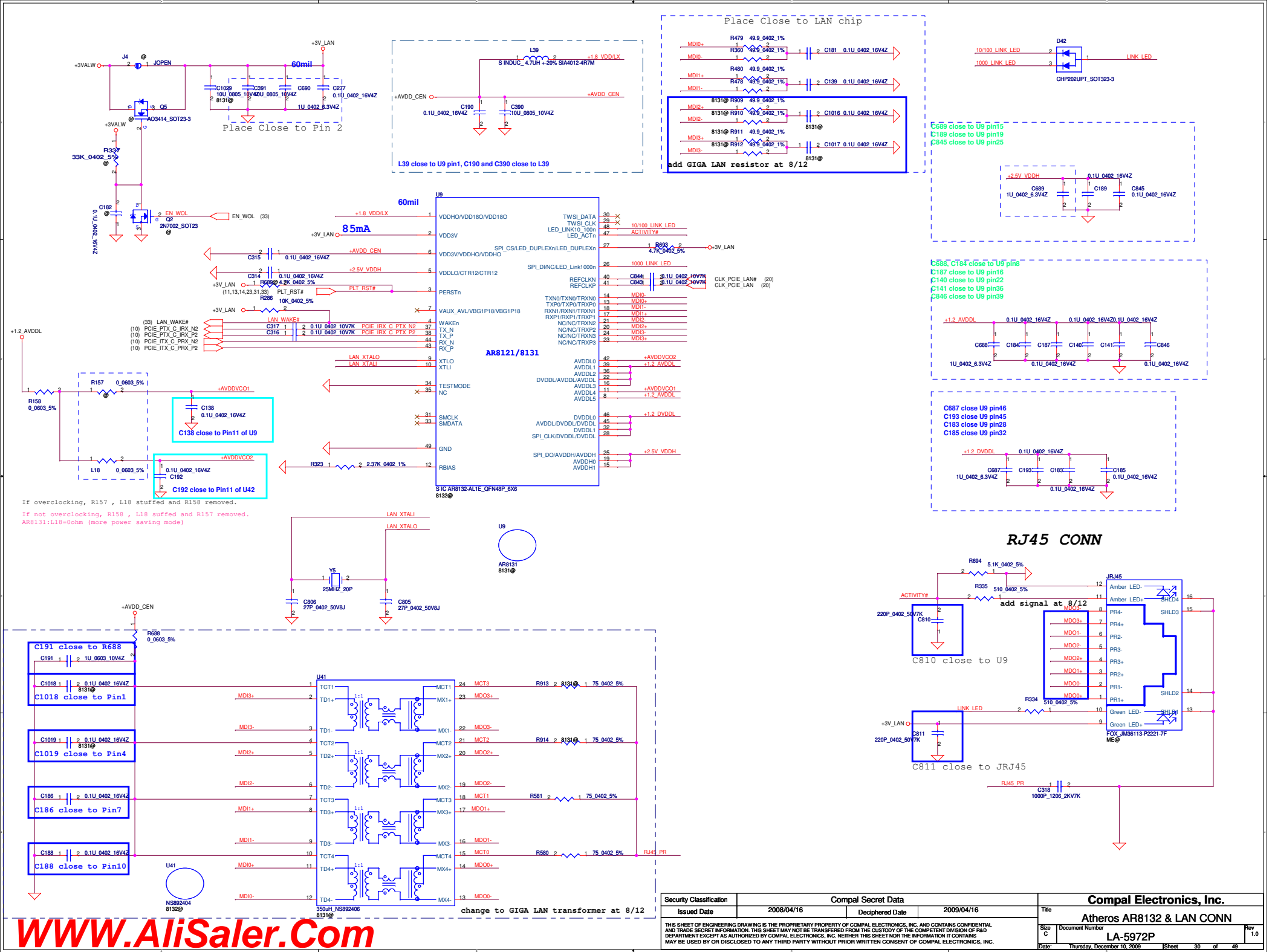
SATA ODD Conn.



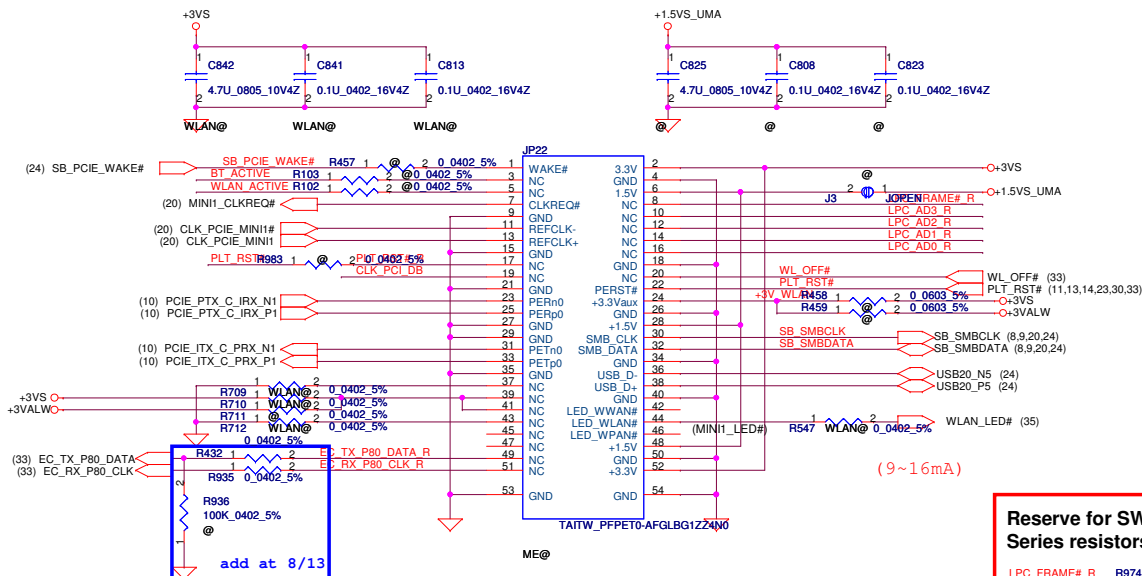
SATA HDD Conn.



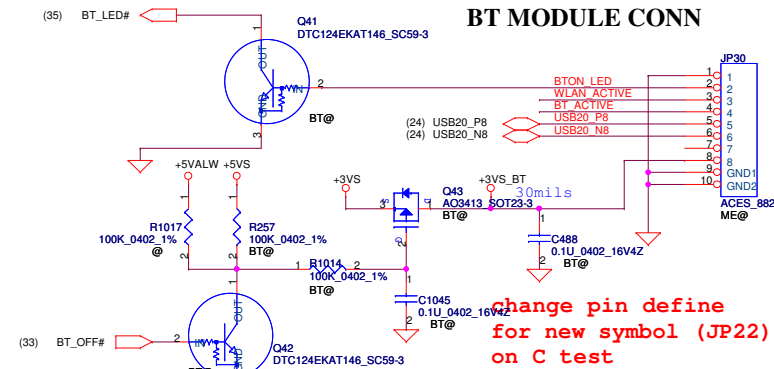
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For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

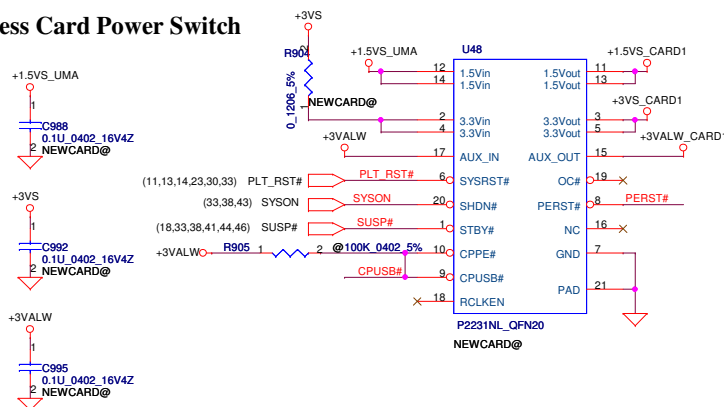


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

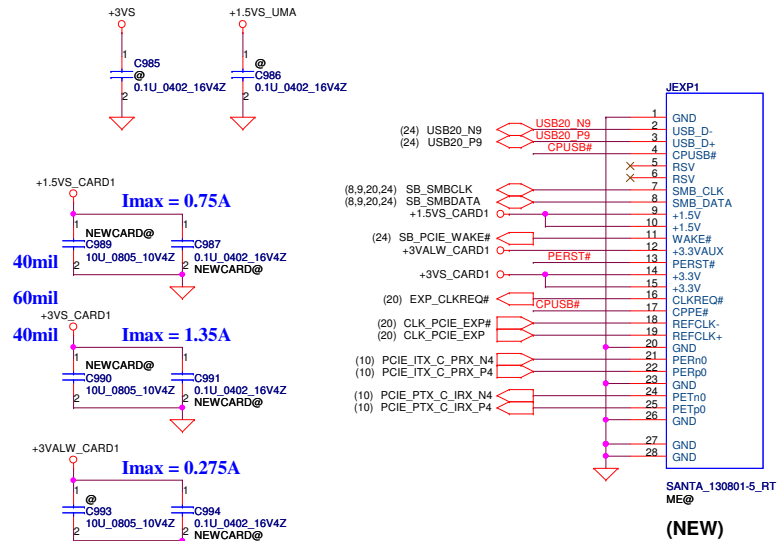
LPC_FRAME#_R	R974	1	2	0.0402_5%	LPC_FRAME#	(23,33)
LPC_AD3_R	R975	1	2	0.0402_5%	LPC_AD3	(23,33)
LPC_AD2_R	R976	1	2	0.0402_5%	LPC_AD2	(23,33)
LPC_AD1_R	R977	1	2	0.0402_5%	LPC_AD1	(23,33)
LPC_AD0_R	R978	1	2	0.0402_5%	LPC_AD0	(23,33)
CLK_PCI_DB	R979	1	2	0.0402_5%	CLK_PCI_DB	(23)

add at 8/11

Express Card Power Switch

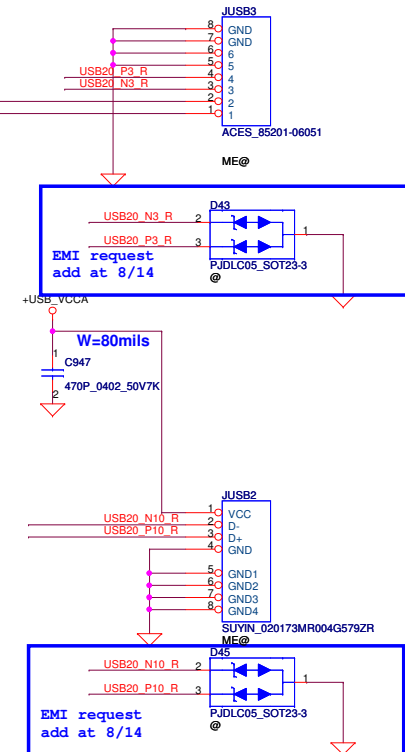
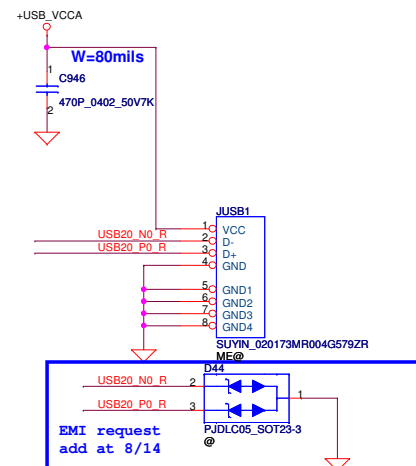
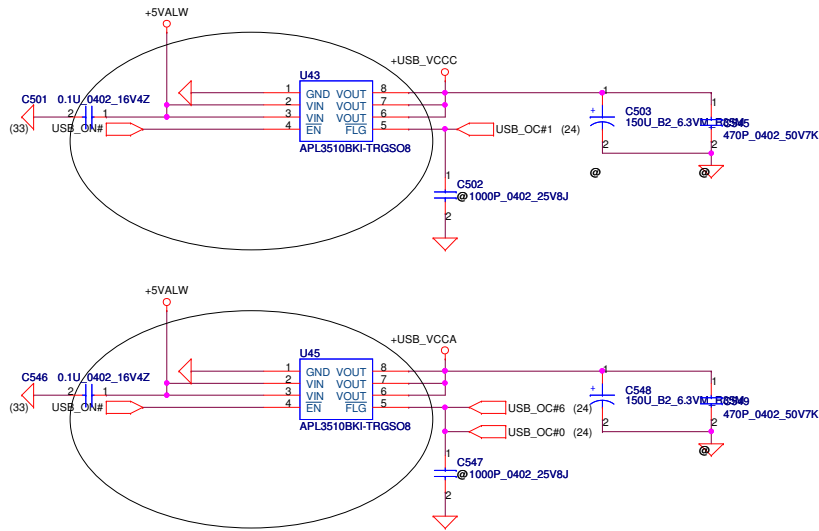
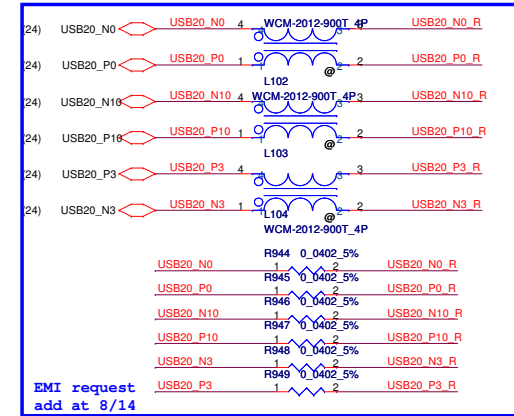
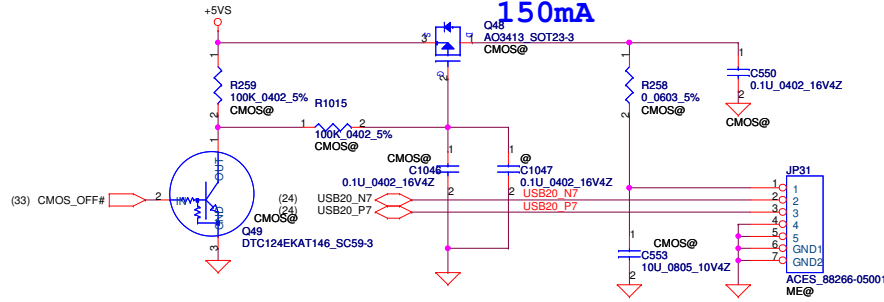


add at 8/11

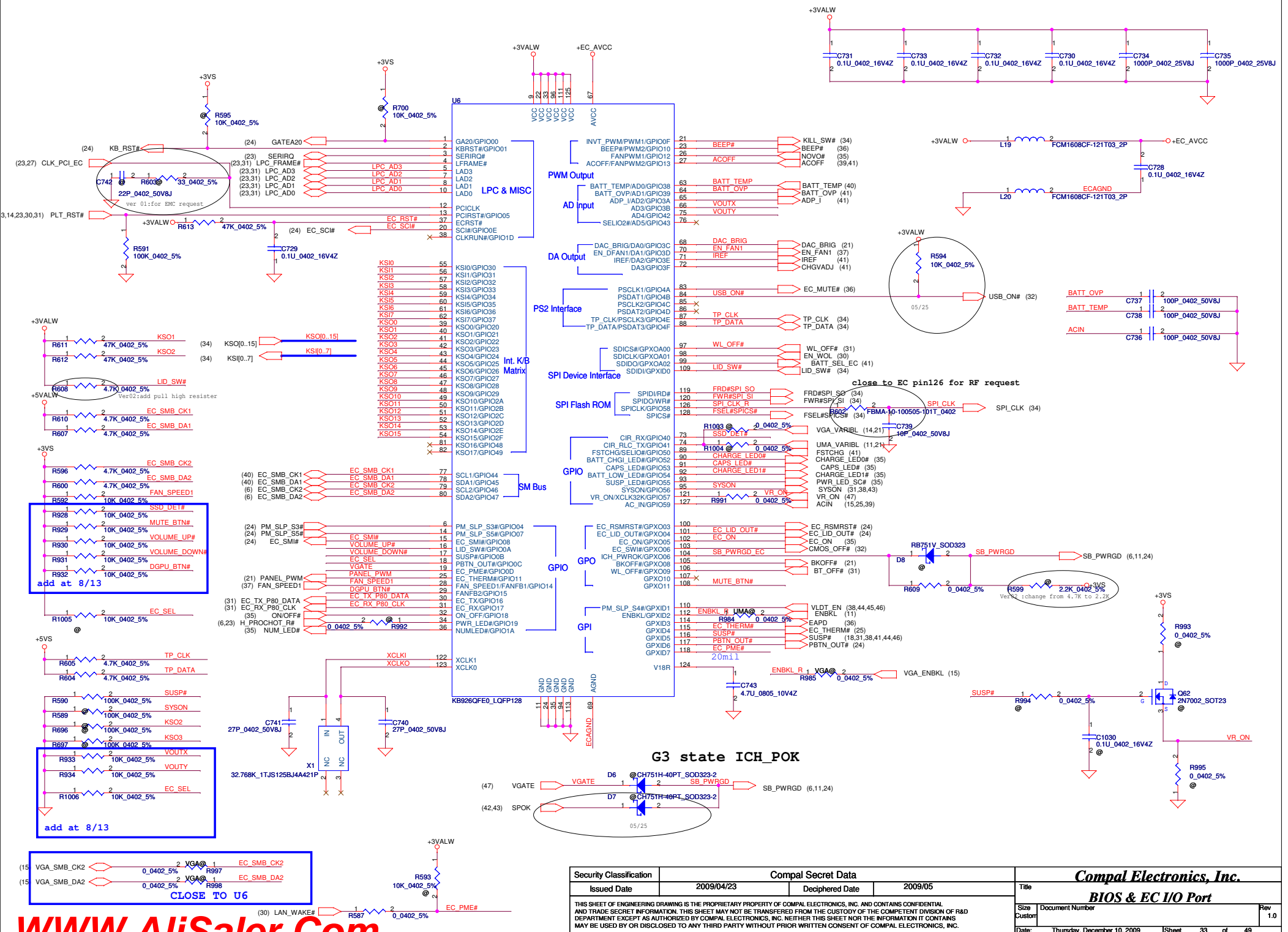


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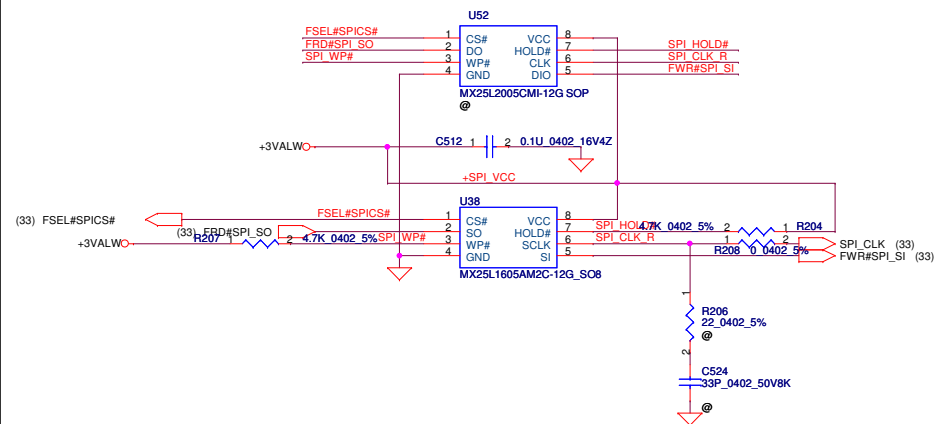
CMOS Camera Conn



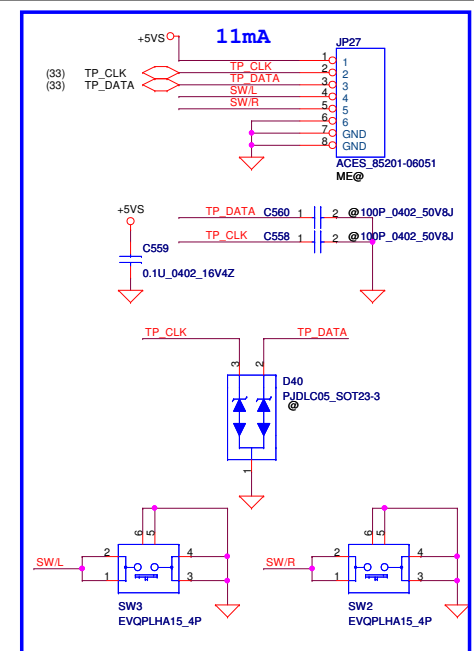
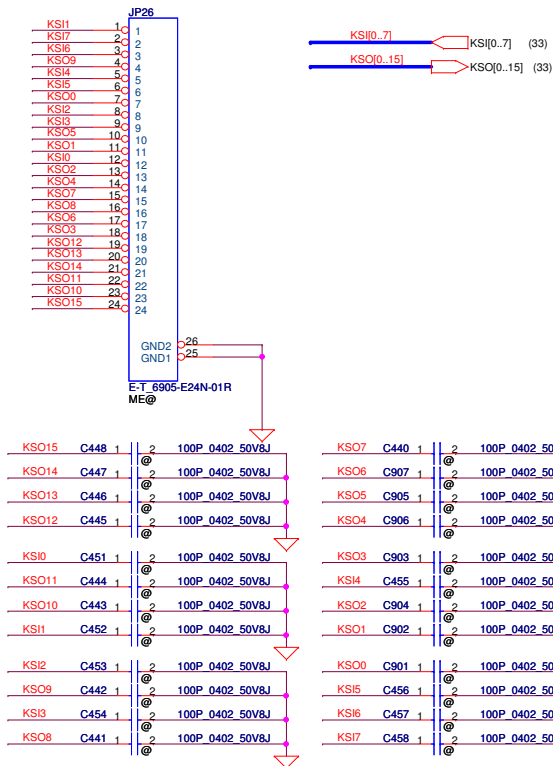
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title
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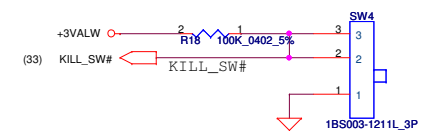
BIOS(SYS / EC / VGA)



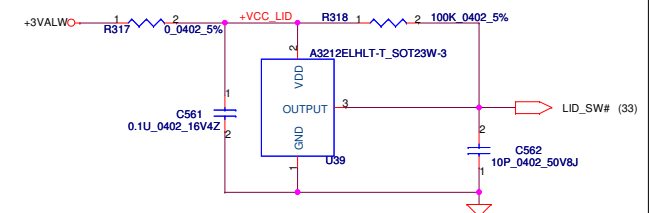
INT_KBD Conn.



Kill Switch

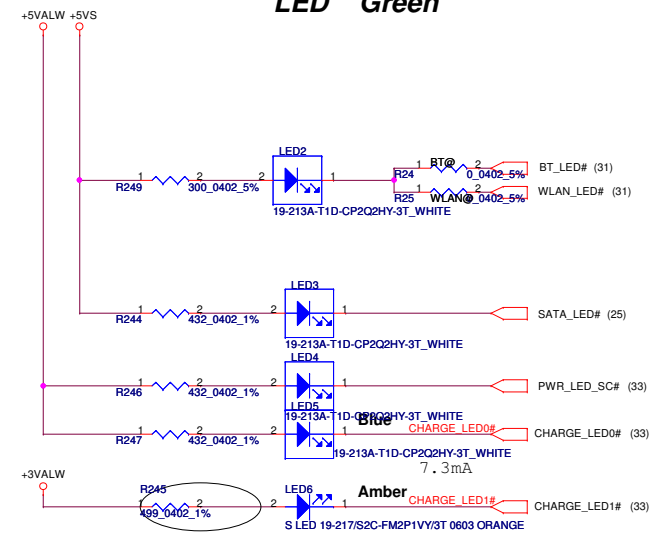
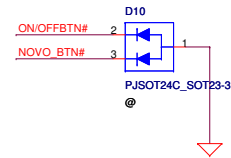


Lid Switch



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ON/OFF switch

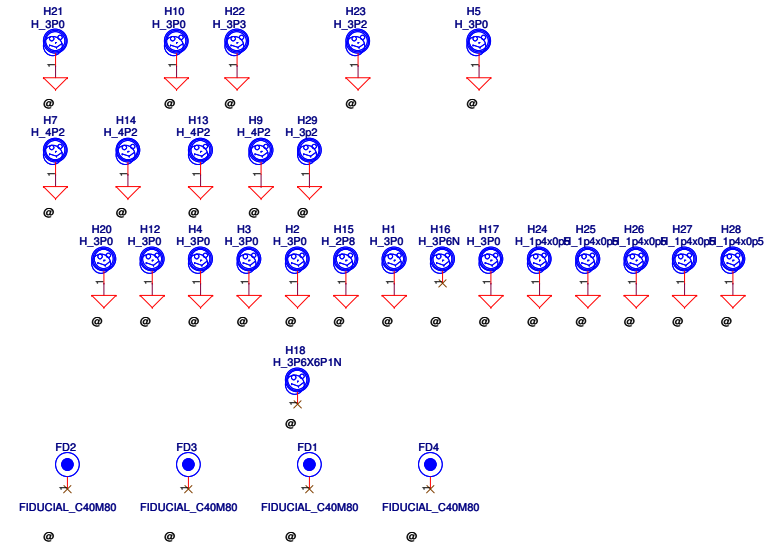
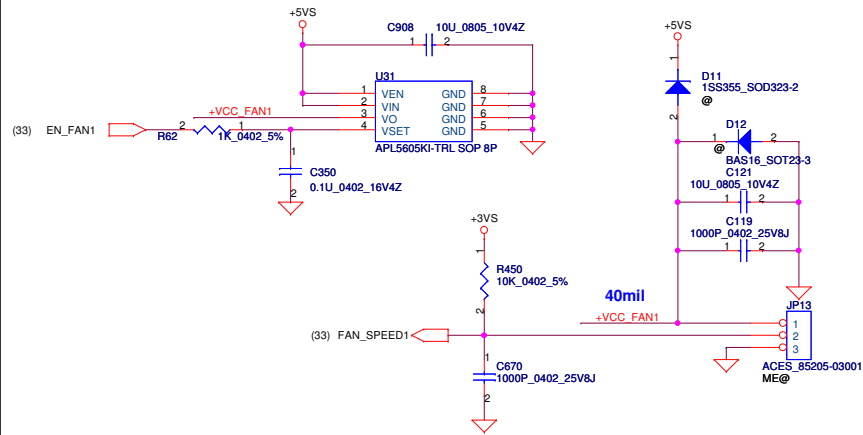


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An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).

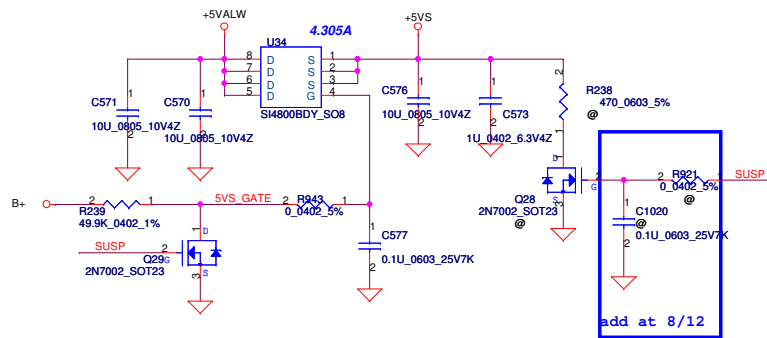


FAN1 Conn

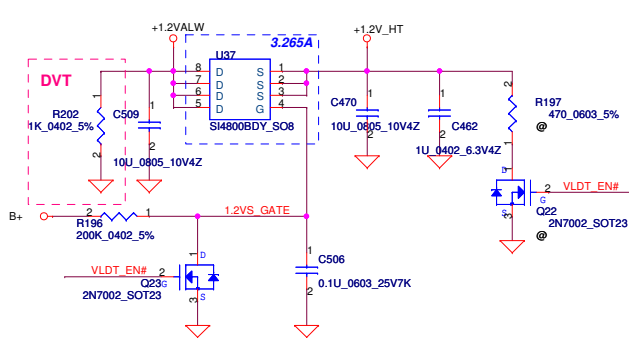


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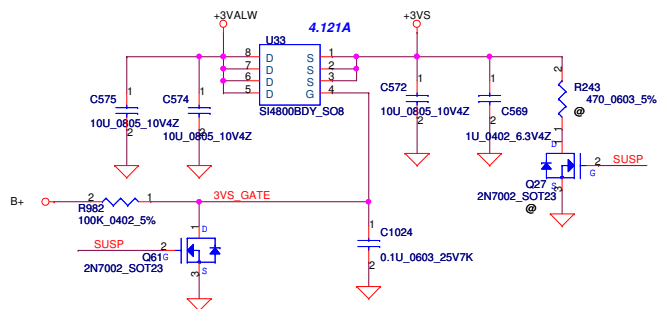
+5VALW TO +5VS



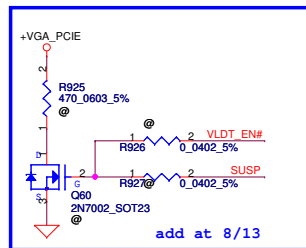
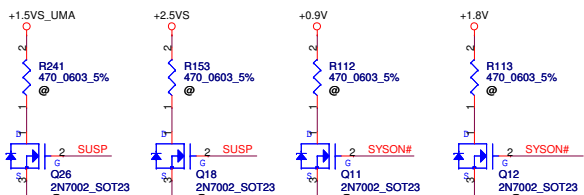
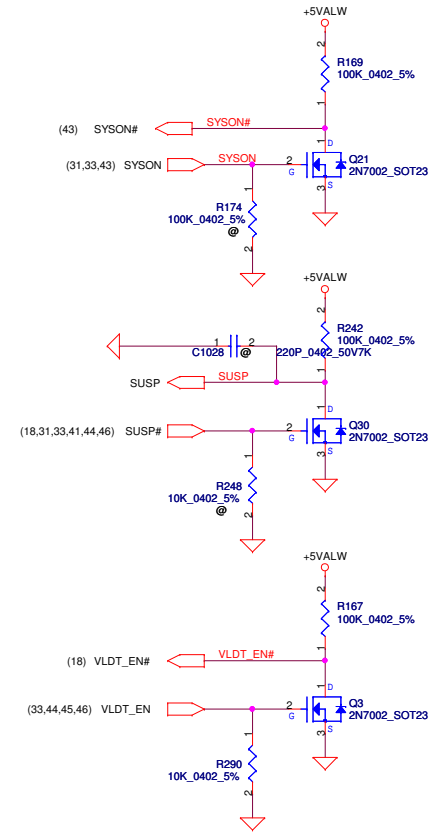
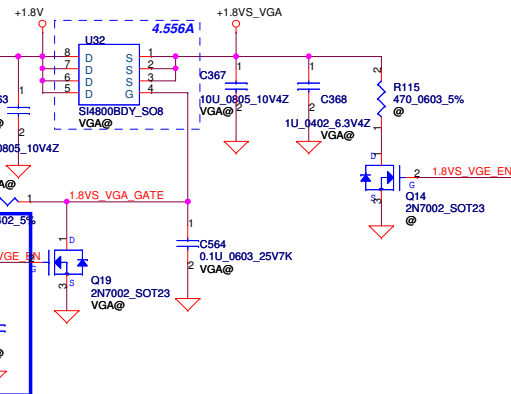
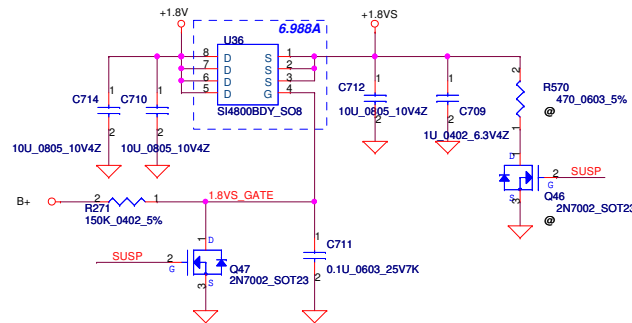
+1.2VALW TO +1.2V_HT



+3VALW TO +3VS



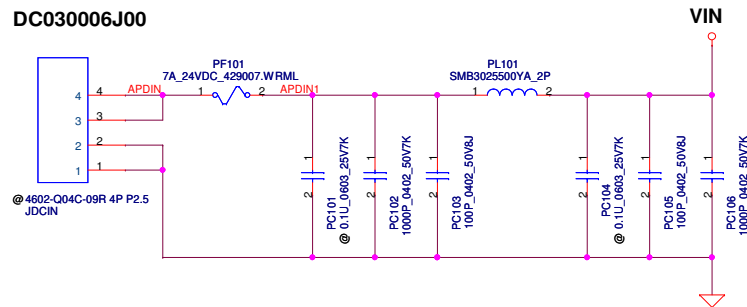
+1.8V to +1.8VS



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				DC Interface	
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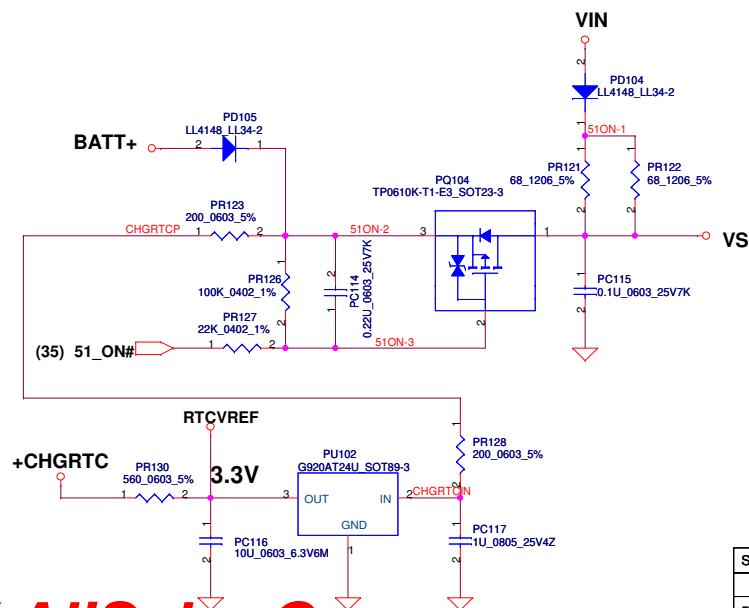
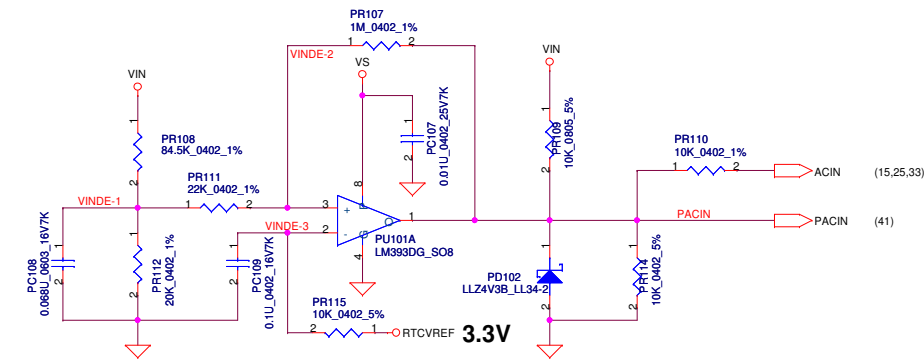
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DC030006J00



Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

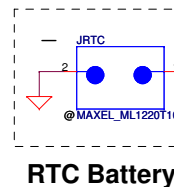
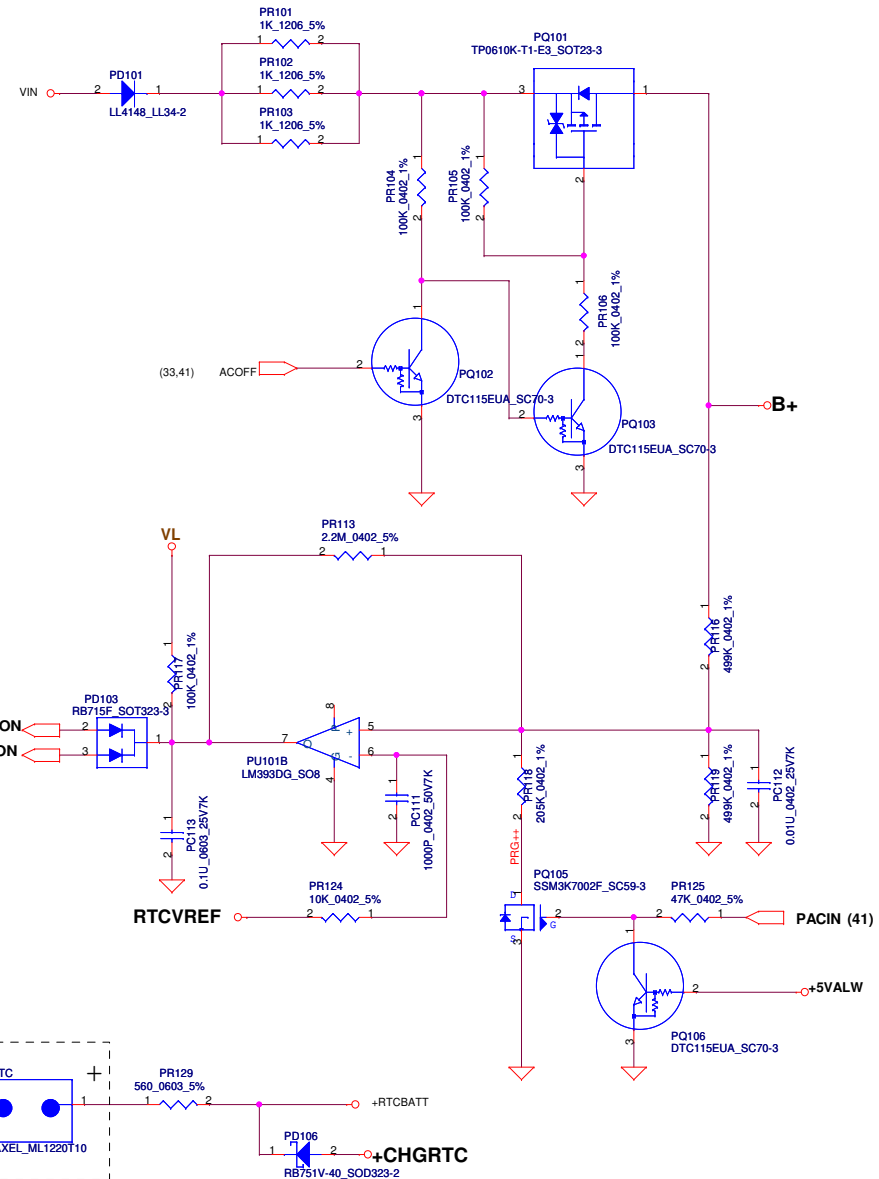


ACIN

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

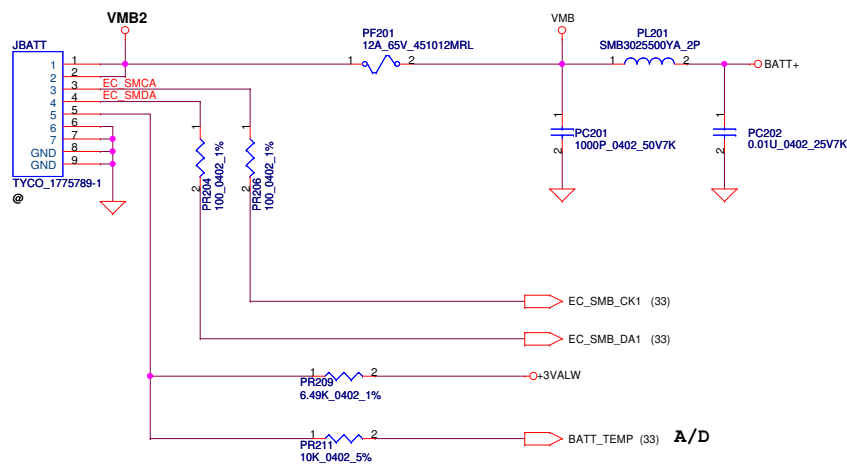
BATT ONLY

	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

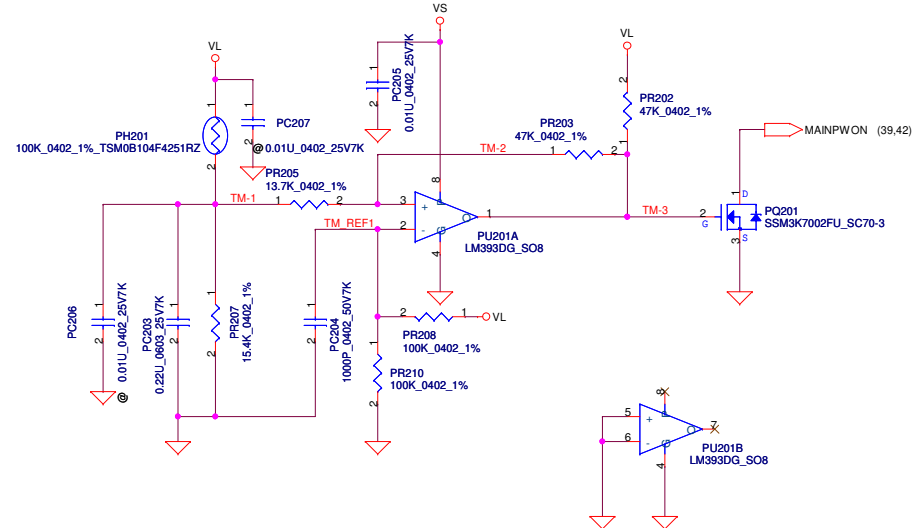


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						Size		Document Number		Rev	
						Custom				1.0	
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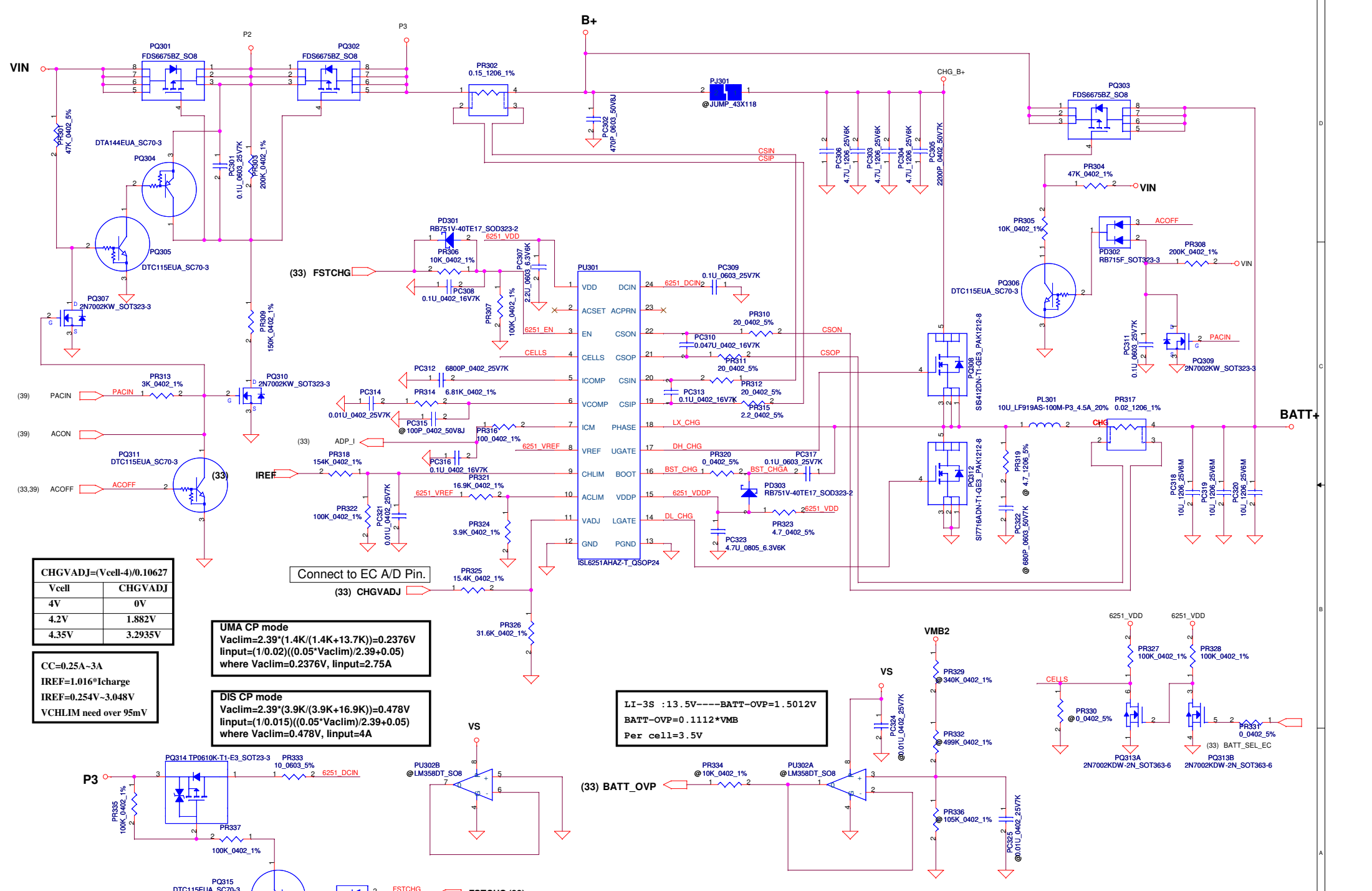
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PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

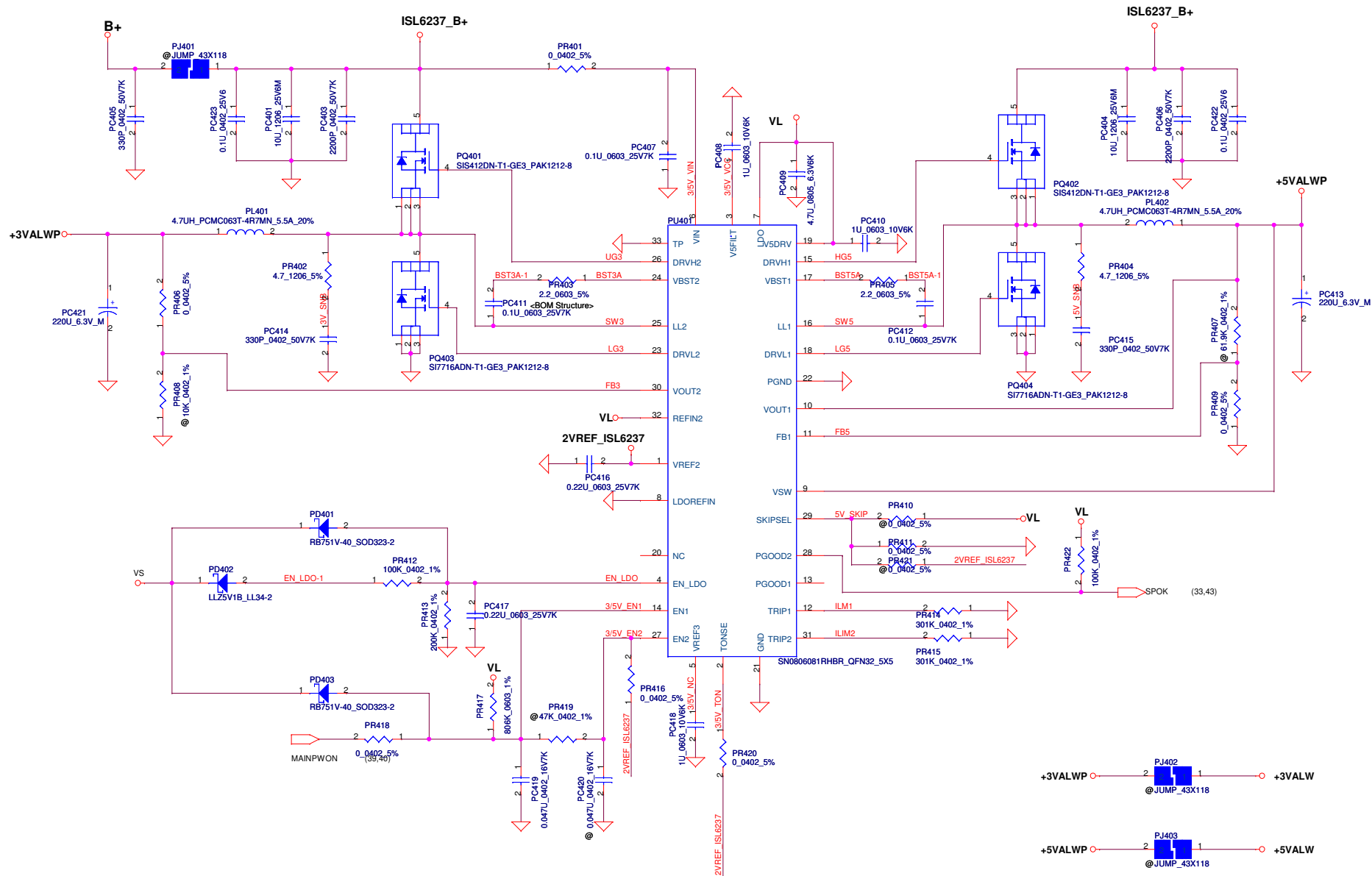
CC=0.25A-3A
IREF=1.016*Icharge
IREF=0.254V-3.048V
VCHLIM need over 95mV

UMA CP mode
 $V_{acli} = 2.39 * (1.4K / (1.4K + 13.7K)) = 0.2376V$
 $I_{npu} = (1 / 0.02) * ((0.05 * V_{acli}) / (2.39 + 0.05))$
where $V_{acli} = 0.2376V$, $I_{npu} = 2.75A$

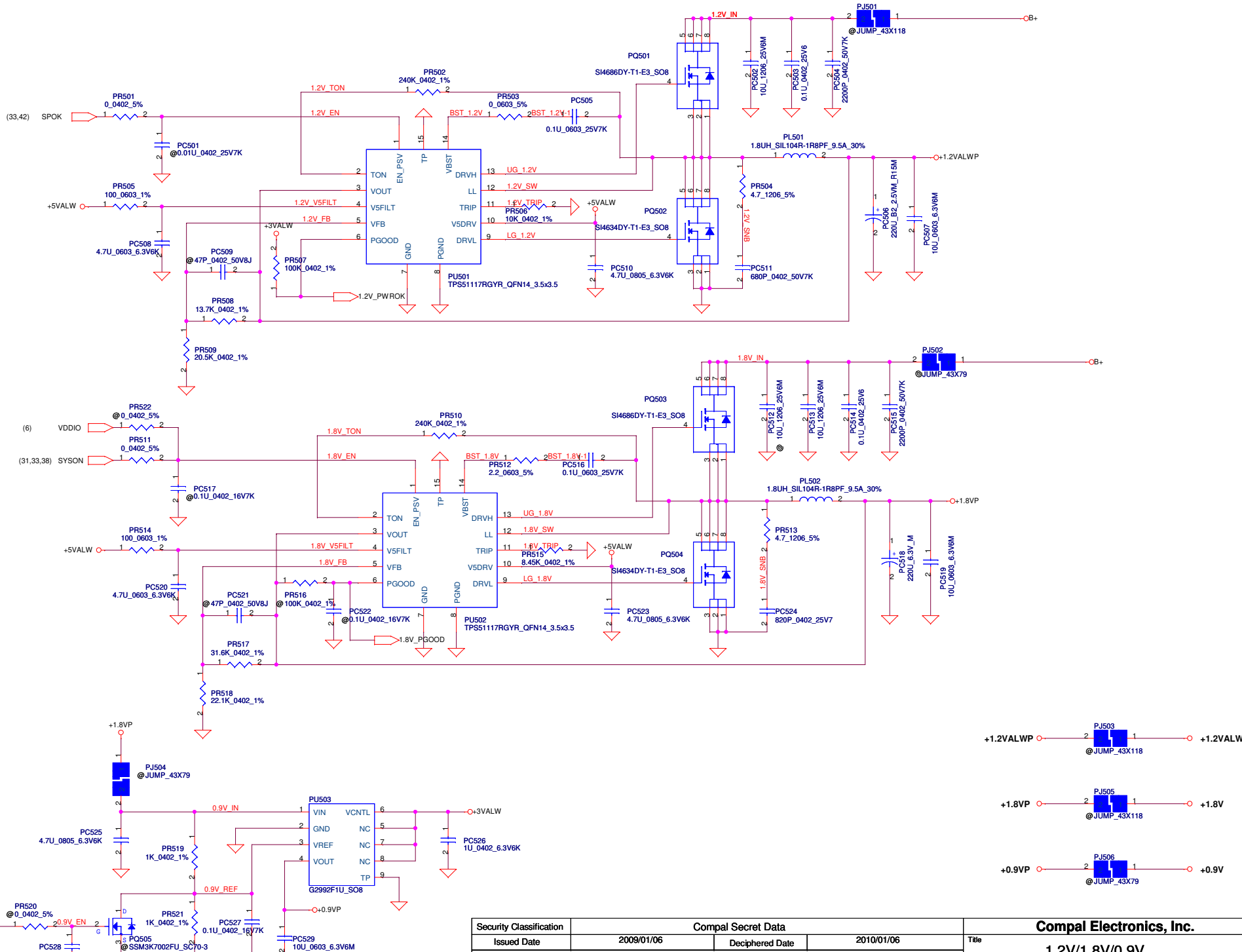
DIS CP mode
 $V_{acli} = 2.39 * (3.9K / (3.9K + 16.9K)) = 0.478V$
 $I_{npu} = (1 / 0.015) * ((0.05 * V_{acli}) / (2.39 + 0.05))$
where $V_{acli} = 0.478V$, $I_{npu} = 4A$

LI-3S : 13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

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2007/6/22		2008/6/22		CHARGER	
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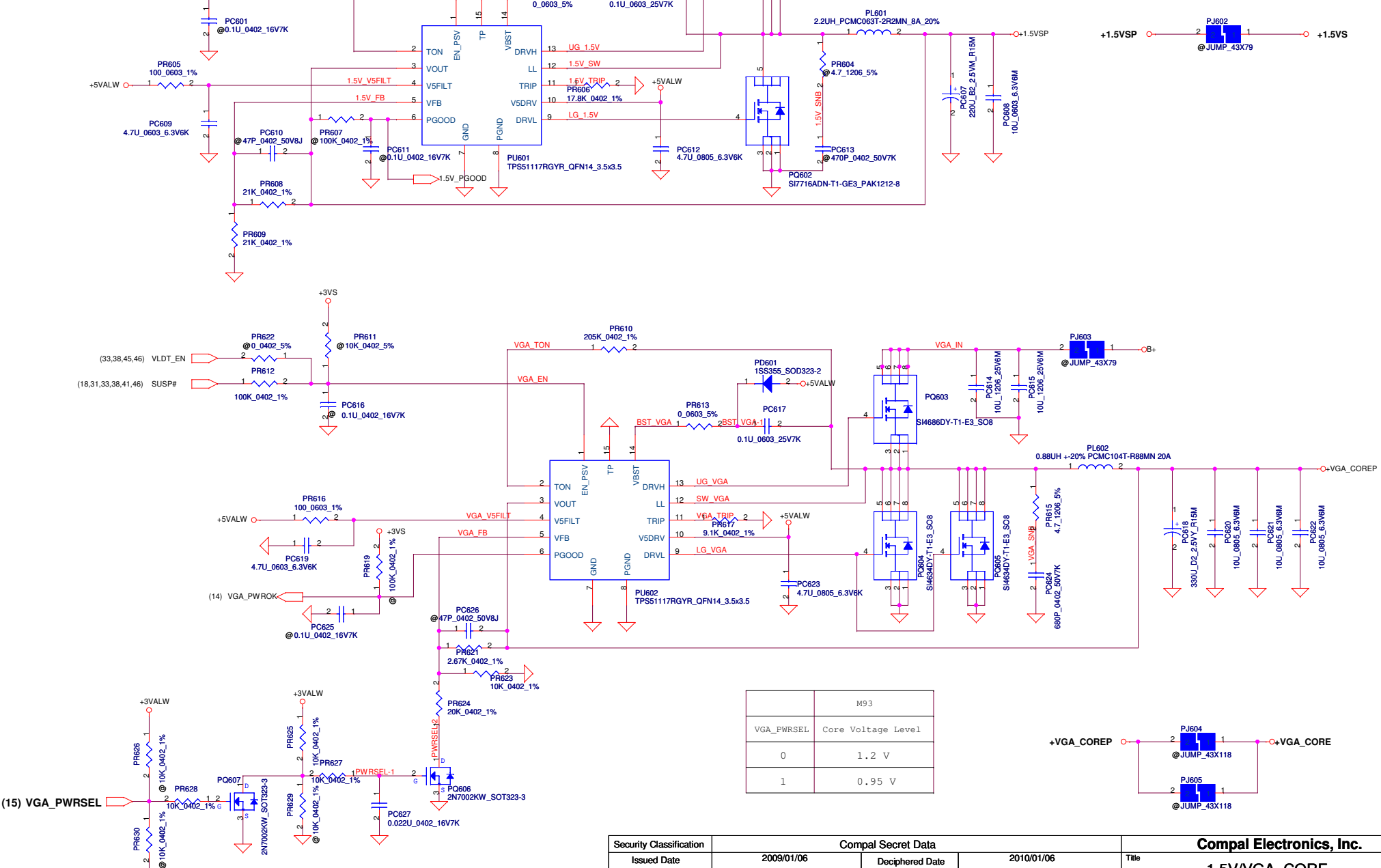


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								1.2V/1.8V/0.9V	
Size		Document Number				Rev			
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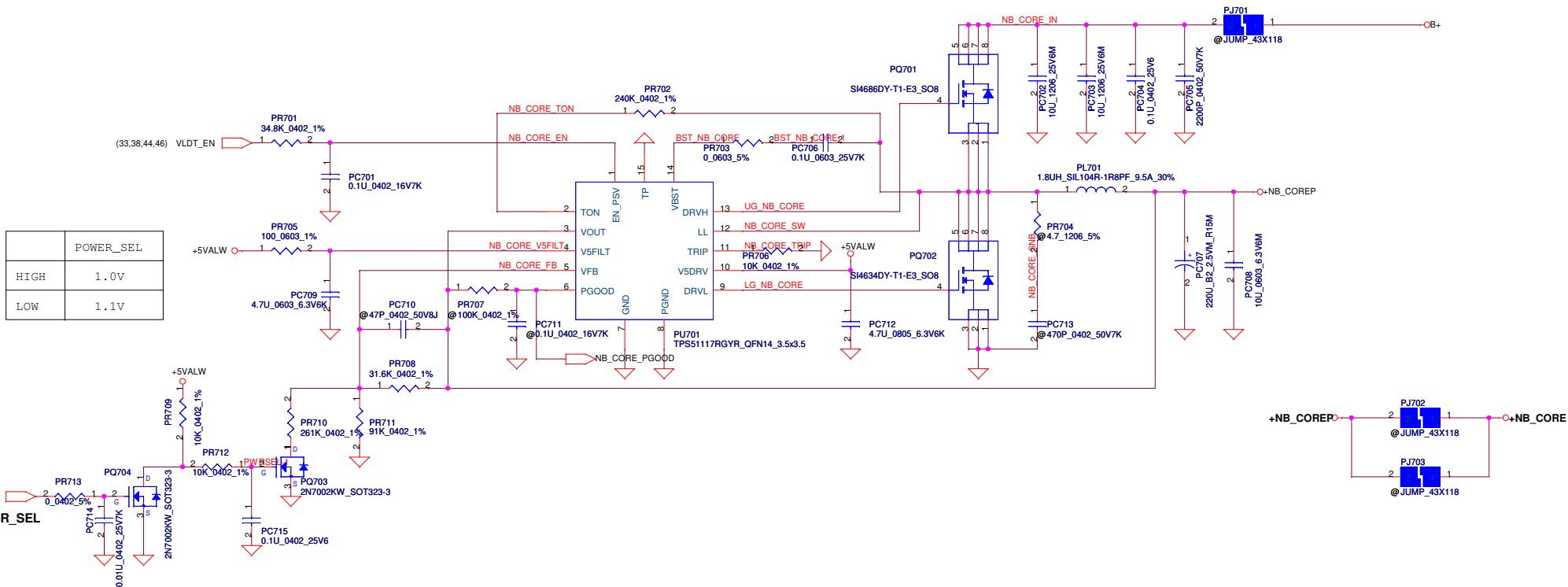
(18,31,33,38,41,46) SUSP#



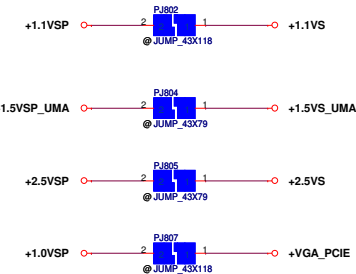
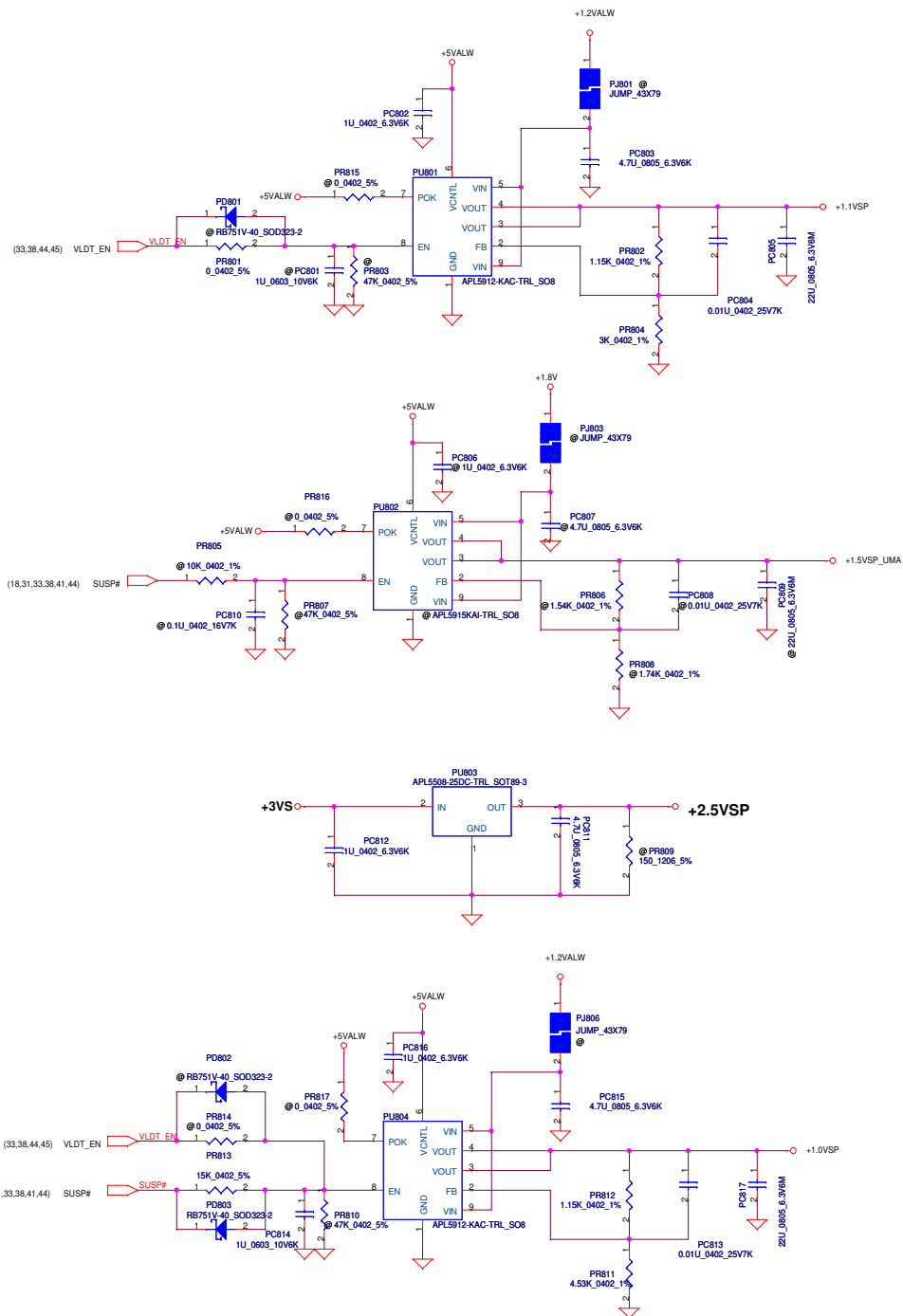
(15) VGA_PWRSEL

	M93
VGA_PWRSEL	Core Voltage Level
0	1.2 V
1	0.95 V

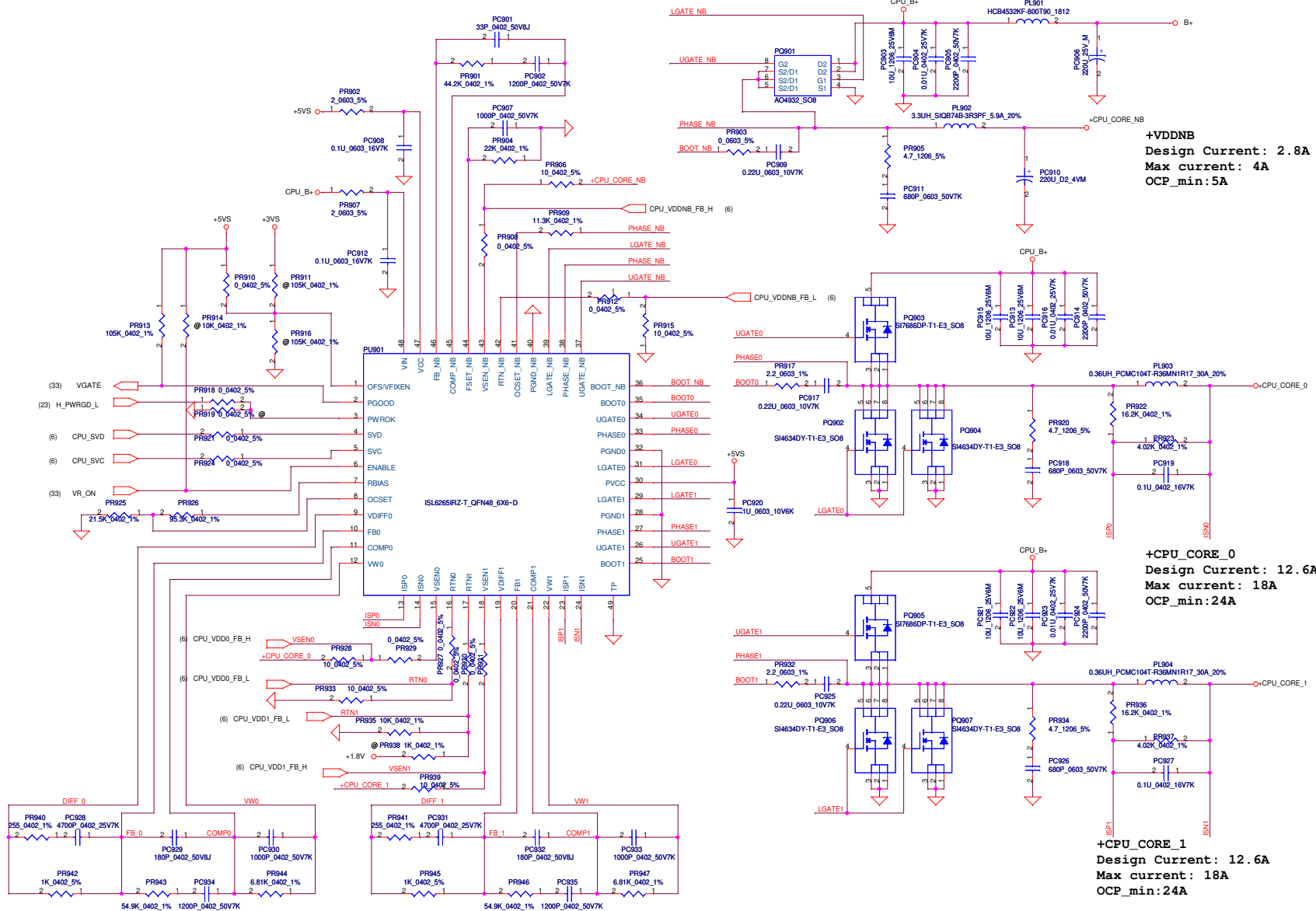
	POWER_SEL
HIGH	1.0V
LOW	1.1V



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Custom				
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	Park	M93
VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K



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Size	Document Number	Sheet	47	Rev 1.0
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Adjust power sequence for VGA_PCIE by HW request	P46	PR831=15K	2009.10.27	EVT
2	Change PC108 from 1000pF to 0.068uF for issue solution	P39	PC108=0.068uF	2009.11.17	PVT
3	Add snubber R & C and modify boost resistor for 1.8VP	P43	PR512=2.2 ohm;PR513=4.7 ohm;PC524=820pF	2009.11.17	PVT
4	Adjust power sequence	P45	PR701=34.8K,PC701=0.1uF Un-pop PR520,PQ505	2009.12.03	PVT
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

- 54321
- D
- C
- B
- A
- 54321
1. change component AP2301GN to AO3413
2. remove R521, R517, R520 and R518, and reserve U49 , U50, R999, R1000, R1001 and R1002 for experiment Vari-bright function.
3. U6.18 add a pull up resistor R1005 and pull down resistor R1006 for check ENE KB926 version.
4. reserve R1003 and R1004 for Vari-bright test.
5. add J8, C1034, C1035, C1036, C1037, C1038 and C1039 for EMI request.
6. Change R583, R584, R585 and R586 Bead from SM010018110 to SM010022410.
7. reserve R1007 for EMI request.
8. Change C633, C640, C662, C948, C660 and C639 to 10pF for EMI rquest.

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